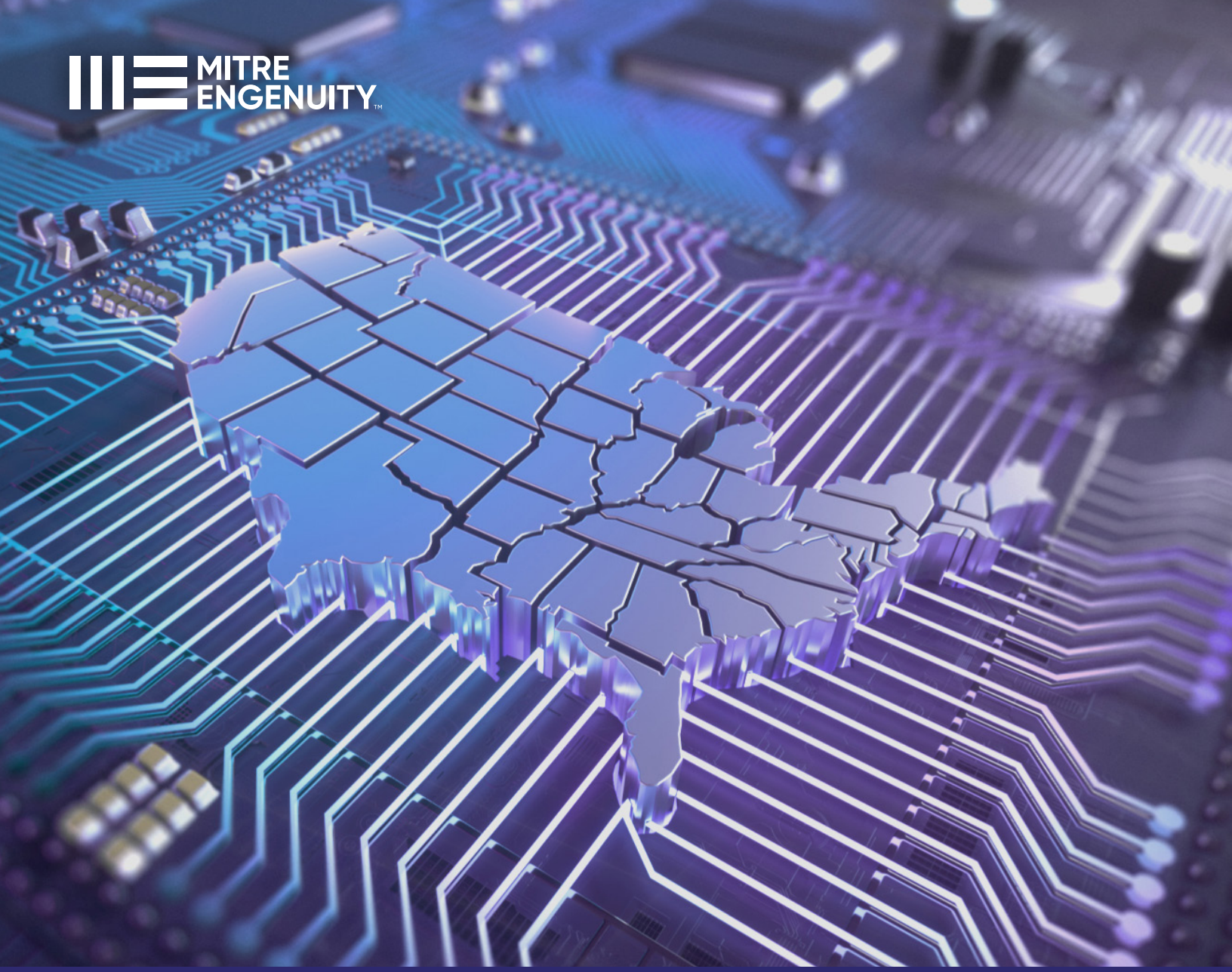

MITRE ENGENUITY™

CREATING AN ENDURING NATIONAL RESOURCE:

A BLUEPRINT FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER AND THE NATIONAL ADVANCED PACKAGING MANUFACTURING PROGRAM

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Contents

Contributors

This position paper ("paper") is a summary of MITRE Engenuity's ongoing work with the industry collaboration it formed in 2021, The Semiconductor Alliance. It represents our efforts to convene and collaborate with industry and university members to develop input and plans for CHIPS activity that will benefit industry and Federal Government objectives. Our first paper, *American Innovation, American Growth: A Vision for the National Semiconductor Technology Center*, was published November 2021 to help inform and shape government CHIPS efforts early on. This was the first collective paper published on the subject and commenced a series of collaborative discussions across the ecosystem. The Semiconductor Alliance continued to convene and grow, to provide a response to the Department of Commerce's March 2022 request for information. We have continued to meet weekly over the past 20 months to develop direction and guidance to support the Department of Commerce and the newly formed CHIPS R&D office. Our working groups have been focused on R&D strategy and planning to guide the portion of CHIPS investments on innovation and design of the chips of the future. This work is relevant to the formation and operation of the National Semiconductor Technology Center and the National Advanced Packaging Manufacturing Program, which will reaffirm America's leadership in semiconductor technology.

The full list of contributors who have agreed to share their names is below.

Masoud Agah, Virginia Tech
Ameen Akel, Micron
Ramakanth Alapati, Yield Engineering Systems
John Allgair, BRIDG
Daniel Armbrust, Silicon Catalyst
Rich Ashooh, Lam Research
Gregg Bartlett, GlobalFoundries
Valeria Bertacco, University of Michigan
Keith Best, ONTO Innovation
Siddharth Bhingarde, Intel
Darren Bischoff, Nano-C
Matthew Blackbourn, Analog Devices
Mark Bohr, Intel
Tom Boone, Western Digital Corporation
Doug Bopp, Vapor Cell Technologies
Clark Britan, MITRE
Jim Browning, Boise State University
Raul Camposano, Silvaco
Bika Carter, GlobalFoundries
Mus Chagal, Great Lakes Crystal Technologies
Preeth Chengappa, Microsoft
Meghali Chopra, Sandbox Semiconductor
Kuntal Chowdhury, BlueFusion
John Cole, MITRE
Ashley Conboy, Lam Research
Mark da Silva, SEMI
Shamik Das, MITRE
Abby Davis, MITRE
Bambi DeLaRosa, Micron
Mike Delaus, Analog Devices
Elaheh Eghbal, MITRE
Raleigh Estrada, MITRE
Keith Evans, Great Lakes Crystal Technologies
Luke Fleet, Kepler Computing
Jeb Flemming, 3D Glass Solutions
Michael Gallagher, DuPont
Laurie Giandomenico, MITRE
Christopher Gilmore, DuPont

Richard Gottscho, Lam Research
Timothy Grotjohn, Great Lakes Crystal Technologies
Carol Handwerker, Purdue University
Ken Hansen, HTKH
Mark Helm, Micron
David Henshall, Semiconductor Research Corporation
Jon Herlocker, Tignis
Todd Holmdahl, Microsoft
David Hopper, MITRE
Mitchell Hsing, InchFab
Gene Irisari, Samsung Electronics America
Subramanian Iyer, University of California Los Angeles
Ajey Jacob, Information Sciences Institute, USC
Raj Jammy, MITRE
Keren Kanarik, Lam Research
Zia Karim, Yield Engineering Systems
Mohamed Kassem, Efabless
John Keating, Synopsys
Lex Keen, SecureFoundry
Chris Keimel, Menlo Microsystems
Liam Kelly, Ambature
Matt Kelly, IPC
Ron Kelly, Ambature
Cliff King, Analog Devices
Jack Kotovsky, Lawrence Livermore National Laboratory
Steve Kramer, Micron
Serge Leef, Microsoft
Luke Lester, Virginia Tech
Shari Liss, SEMI Foundation
Gino Manzo, Virginia Microelectronics Consortium
Eric Martin, MONSTR Sense Technologies
Mike Mayberry
Mark Melliar-Smith, Canon Nanotechnologies
Ian Melville, GlobalFoundries
Samir Mittal, Micron
Jeremy Muldavin, GlobalFoundries
Haritez Narisetty, GlobalFoundries
Jawad Nasrullah, Palo Alto Electron
Joe Pasetti, imec
Monita Pau, ONTO Innovation
Steve Pawlowski, Micron
John Pellerin, GlobalFoundries
H.-S. Philip Wong, Stanford University
Praneetha Poloju, Microsoft
Jonathan Prange, MITRE
Nick Pugliano, DuPont
Siddharth Rajan, The Ohio State University
Alon Raphael, Femtometrix
Wally Rhines, Cornami
David Robertson, Analog Devices
Jeffrey Rogers, Lam Research
Tom Rucker, Intel
Sam Salama, Hyperion
Gurtej Sandhu, Micron
Erin Schultz, MITRE
Rahul Sen, Nantero
Nitin J. Shah, MITRE
Willy Shih, Harvard Business School
Emily Smith, MITRE
Moise Solomon, MITRE
Veronika Stelmakh, Mesodyne
Adam Stieg, University of California Los Angeles
John Terry, Espre Technologies
Kirk Thompson, MITRE
Gilroy Vandentop, Intel
James Vandevere, BRIDG
Dan Walters, MITRE
Glen Wilk, ASM
Michael Wishart, Efabless
Eric Witherspoon, Applied Materials
Todd Younkin, Semiconductor Research Corporation
Ray Zanoni, Raytheon Technologies
Ming Zhang, Synopsys
Victor Zhirnov, Semiconductor Research Corporation
John C. Zolper, Raytheon Technologies
Zoran Zvonar, Analog Devices

Introduction | Executive Summary

The stage is set for a historic resurgence of U.S. semiconductor leadership. Congress has appropriated over $50 billion to fund the provisions of the CHIPS Act, including the National Semiconductor Technology Center (NSTC) and the National Advanced Packaging Manufacturing Program (NAPMP). Galvanized by this substantial government investment and growing threats to U.S. competitiveness, industry is preparing to make significant investments of its own. Since 2020, nearly 40 companies have announced approximately $200 billion in planned investments to create new semiconductor production capacity and to strengthen the semiconductor supply chain in the U.S. [1; 2]

However, while these numbers show great promise, they alone do not ensure success. With both adversaries and allies making comparable – or even greater – investments in growing their own domestic industrial bases, the challenge becomes not who can invest the most, but who can invest the most strategically. [3; 4] The race for leadership in the global semiconductor industry is a marathon, not a sprint. As in any long race, winning is a matter of consistency, endurance, and strategy. Bursts of energy, like the one that the U.S. semiconductor ecosystem is currently experiencing, can propel a contender to the head of the pack, but that advantage will only last if the contender can put forward the effort needed to capitalize on it.

In this paper, MITRE Engenuity and The Semiconductor Alliance explain how the U.S. can ensure that the NSTC – in conjunction with the NAPMP and in collaboration with the Department of Defense (DOD) Microelectronics Commons and the National Institute of Standards and Technology (NIST) Manufacturing Institutes – becomes an enduring national resource that advances U.S. leadership for decades to come. We build on the themes and recommendations expounded in our November 2021 paper, *American Innovation, American Growth: A Vision for the National Semiconductor Technology Center*, and translate our vision into a detailed blueprint for how the U.S. can make the most of its present surge in investment. [5]

We contend that there are four key points to creating an NSTC that delivers lasting impact:

1. **Establishing Effective & Inclusive Governance**

   To achieve its ambitious vision and to foster a thriving domestic ecosystem, the NSTC governance model needs to balance inclusivity, effectiveness, and efficiency. NSTC stakeholders will be diverse – ranging across federal, state, and local government, startups, mid-sized firms, large multinational corporations, educational institutions, national laboratories, the defense industrial base, etc. To lower barriers to participation and to drive growth in the innovation ecosystem, the NSTC must ensure that all segments of its stakeholder base have a voice.

   At the same time, the NSTC needs to keep its board of directors and other key advisory bodies neutral and balanced to prevent narrow interests from dominating decision-making at the expense of the greater good. The NSTC must also keep such bodies small and agile enough to make timely, strategic decisions. In this paper, we provide detailed recommendations for the structure and composition of the NSTC's advisory bodies (board of directors, Technical Advisory Committees, and executive team) and its relationship to the NAPMP, as well as for the optimal distribution of decision-making authority and strategies to ensure that the NSTC evolves to keep pace with the rapidly changing ecosystem it will serve.

   In addition to discussing the NSTC's governance structure, we touch on the subject of defining, measuring, and ensuring accountability for success. The NSTC will have ambitious, complex objectives. It will translate American innovation into American growth by creating pathways that bring revolutionary technologies from lab to fab, all within the domestic ecosystem. It will also promote U.S. national security by increasing access to critical technologies and fostering a flourishing domestic startup ecosystem. Furthermore, it will help to train a robust semiconductor workforce of the future.

   An important step toward achieving these objectives is to define what it means to succeed with respect to each and how to measure that success; this will ensure NSTC leadership can be held accountable. In this paper, we discuss how

the Department of Commerce (DOC) and NIST should create success criteria to hold NSTC leadership accountable; we also consider ways that the NSTC leadership, in turn, can orient its programs toward success for the nation.

2. **Setting an Ambitious, High-Impact Technology Agenda**

   In order to sustain and grow the support, participation, and investment of its stakeholders, the NSTC should facilitate revolutionary, market-shaping technological advancements that strengthen U.S. economic leadership and national security. That is, its technical output must be high-impact and inspiring. Therefore, the NSTC should pursue Breakthrough Challenges – ambitious, and revolutionary, and actionable R&D and prototyping technology programs. To achieve these pursuits, the NSTC will need a robust set of experts, as well as effective frameworks, criteria, and repeatable processes for selecting its Breakthrough Challenges. These experts, frameworks, criteria, and processes will need to guide the NSTC toward investing in challenges that drive innovation across the full-stack and unite the best minds in the U.S. around shared, hard problems. By engaging broadly and strategically across the ecosystem, the NSTC will be able to define Breakthrough Challenges that will have high market impact and substantial importance to U.S. economic competitiveness and national security. In this paper, we describe how the NSTC ought to leverage its Technical Advisory Committees to distill the most pressing market and technological challenges of the coming decades and use the information to create compelling, galvanizing Breakthrough Challenge programs that will propel U.S. innovation and leadership.

3. **Creating a Robust Network and Operating Model for Executing Technical Agendas**

   The long-term success of the NSTC's technical programs – and, thus, the support of the NSTC's stakeholders – will depend on the organization's ability to execute its agenda both effectively and efficiently. To make progress quickly, the NSTC should take advantage of a network of existing facilities and capabilities rather than wait for new ones to be created. It should also build strategic partnerships to leverage complementary capabilities in allied nations. Over time, it will be critical that the NSTC continue to augment this initial network

by creating new "enabling capabilities" (e.g., tools, test vehicles, baselines, metrology, and characterization, etc.) that stay ahead of market needs, lower barriers to innovation for all participants, and catalyze the development of revolutionary technologies.

The NAPMP will play a crucial role in establishing the enabling capabilities needed for securing leadership in advanced packaging. In order to execute substantial, complex technical programs across a large and evolving network of distributed facilities, the NSTC will need world-class program management that can handle not only the logistical elements of work execution, but also ensure that programs are truly "full-stack" by building connections across different aspects of the NSTC's work. This same world-class program management will also be key to ensuring that, as the focal point of the U.S. semiconductor innovation ecosystem, the NSTC is able to coordinate and to collaborate effectively across all CHIPS programs and drive a whole-of-nation approach to accelerating innovation. In this paper, we detail what the NSTC's infrastructure and capability network should look like, how it should function, and how program management teams can ensure that the NSTC is able to leverage all available resources effectively to achieve its mission.

4. Ensuring Long-Term Financial Sustainability

The NSTC will have a responsibility to the nation to be a good steward of taxpayer resources; it can do this by ensuring that it creates as much impact as possible with the catalytic funding it receives from the CHIPS Act. To create this impact, the NSTC should create value and diversify its income to include substantial private revenue and state/local sources. Existing organizations in the global semiconductor ecosystem provide several examples of ways the NSTC could do so. However, past precedents also illustrate that the goal cannot and ought not be that an organization like the NSTC achieve 100% financial self-sufficiency, relying only on earned revenue with no government funding. The highly capital-intensive nature of the semiconductor industry and the rapid pace at which tools and other enabling technologies evolve mean that the NSTC will require long-term funding commitments from both private and public-sector stakeholders. Even imec, which has been an invaluable resource to

semiconductor companies worldwide for decades, still relies on government funding to supplement its operating income. [6] In this paper, we recommend various ways that the NSTC can diversify its income streams and set reasonable expectations for the long-term investment the NSTC will need to be sustainable.

Armed with these recommendations, the DOC and NIST will be well-prepared to establish an NSTC that has a governance structure that ensures accountability for achieving its mission, the ability both to set and to execute a revolutionary technology agenda, and a financial underpinning that ensures longevity. The U.S. is competing in a marathon where gaining an edge is just as much a matter of how much energy and resources contenders have as it is about how they choose to expend them. As the focal point of the U.S. ecosystem, the NSTC will be able to coordinate across the full set of public and private investments to ensure that the U.S. leverages its energy and resources to maximum advantage. With focused strategic planning and sound execution, the NSTC will be an enduring national resource that enables the U.S. to surge ahead – and to stay ahead – in the heated race for leadership in the global semiconductor industry.

Establishing Effective and Inclusive Governance

The passage of the CHIPS and Science Act presents a unique opportunity to catalyze American leadership in semiconductor technologies and manufacturing that are critical to our economic and national security. A neutral and resilient governance model for the NSTC is critical to capitalizing on this opportunity. The NSTC should define its technical, execution, and investment priorities in a way that accounts for the needs and perspectives of a large, diverse set of stakeholders without being beholden to or unduly biased by any of them. The Semiconductor Alliance has created the following set of principles by analyzing best practices of public-private partnerships and the NSTC's governance model should strive to uphold them:

NEUTRALITY	Ensure the NSTC delivers on its objectives and provides value to its members by selecting leadership free of conflicts and vested interests.
AGILITY	Empower the NSTC's leadership to make decisions that accelerate the domestic R&D agenda and support them by minimizing complexity wherever possible.
EXPERIENCE	Convene the ecosystem's best engineers, scientists, technologists, and product managers to solve complex problems.
DYNAMISM	Improve and evolve through regular assessments of progress towards objectives; continuous adoption of new concepts and capabilities; refresh leadership perspectives and capabilities regularly.
INCLUSIVITY	Lower barriers through collaborative and pre-competitive R&D, enabling the domestic ecosystem to leverage NSTC resources; clear and firm IP frameworks to facilitate the trust required for inclusivity.

The long-term success and financial sustainability of the NSTC will depend largely on a commitment to its mission and the value it provides for its members. Growing the support of key stakeholders will be a natural byproduct of the strength of its orientation towards public good, strategic vision, neutral governance, and decisive action. Collaboration across the ecosystem is essential: the U.S. government is committed to providing leadership and seed capital as it incubates the NSTC; industry must provide insight and technical guidance on market demand signals and manufacturing needs; startups must leverage resources to commercialize disruptive technology and business ideas; academia must bring its deep scientific understanding and world-leading workforce development capabilities; and national laboratories and defense companies must bring their one-of-a-kind capabilities and government use cases. As the NSTC is created, DOC and NSTC leadership must align these entities through common interests to create an enduring resource for the nation.

As mandated by the CHIPS Act, the NAPMP is a program led by the Director of NIST in coordination with the NSTC. It is a concerted effort directed towards improving the U.S.'s advanced packaging capabilities and this is crucial for U.S. economic and national security and domestic supply chain resiliency. Advanced packaging today is a scaling vector for technology which cuts across all parts of the stack and must be given a disproportionate share of investment. However, full-stack innovation depends on closely coupled advanced packaging and semiconductor technology development. The CHIPS R&D program at NIST should charter the NSTC to manage the NAPMP. Leveraging the NSTC's governance and organizational capabilities, including assigning an executive responsible for the program,

will ensure cohesion between semiconductor fabrication and advanced packaging R&D agendas, reduce management overhead, and avoid complex coordination that would otherwise need to be developed. The recommendations that pertain to managing the NAPMP are further described herein.

Non-Profit Corporate Structure, Independent Board of Directors, and Executive Management

The CHIPS Act in the 2021 National Defense Authorization Act mandates that the NSTC is an independent public-private partnership. The DOC has created a CHIPS R&D office to incubate, define, and establish the NSTC. In line with DOC's public statements, the NSTC should be a non-profit organization with its own bylaws, governance, and board of directors. To ensure neutrality, no single entity, group, technology, region, or market should have a dominant voice in its management. As a non-profit, mission success will drive NSTC's operations to deliver on the objectives laid out in the CHIPS Act.

The board of directors should be the primary oversight function which ensures that the NSTC executes its mission and upholds its core principles. The board should consist of 15 members with a deep understanding of semiconductor ecosystem needs. Board member responsibilities should be consistent with that of a neutral and independent board, which includes upholding the national objectives of the NSTC through its strategy and fiduciary oversight, audit, compensation, and security, and not the objectives of any other organization, such as an employer. Board members should be selected for their significant expertise and c-suite or comparable experience in academia, industry, and national laboratories. The board should consist of an independent chairperson, a chief executive officer (CEO), and individuals with expertise from the following areas:

- 4-5 Integrated Circuit Manufacturers, Design Firms, and End System Makers
- 2-3 Semiconductor Equipment, Material, Electronic Design Automation, and IP providers
- 2-3 Universities
- 1 National Lab
- 1 Defense Industry
- 1 Startup Ecosystem (e.g., serial entrepreneur, entrepreneur-turned-investor, or individual who can represent these interests)
- Federal government representatives from DOC and DOD, as determined by appropriate government stakeholders

All government representatives should be senior officials (e.g., directors) with subject matter background and responsibility for relevant technical R&D, procurement, or workforce programs. Regional and state representatives as well as political appointees should not be on the board but can be regularly engaged and briefed. At its discretion, the board should create sub-committees that monitor the different operational aspects and success metrics of the NSTC.

The chairperson of the board must be someone who has considerable semiconductor industry, technology, and business experience. This person must be free of conflicts of interest associated with financial or regional motivations, have a balanced perspective, and understand the needs of the ecosystem. The chairperson should guide the board towards making decisions that help the NSTC achieve its stated objectives and provide guidance to the executive management team.

To evolve with technology, markets, and business, the NSTC and its board must reflect the semiconductor ecosystem as it changes over time. Board members should have fixed terms of three years or less, with an initial staggered tenure, such that there is always a mixture of new and established

members. New board member nominations should reflect the changes in the NSTC's technology focus areas, markets, and priorities. There should be clear guidelines for transition and succession planning for new board members. The board should conduct periodic reviews of performance to ensure the NSTC is adhering to its mission, delivering on national objectives, and providing value to the ecosystem. The NSTC should hire a dedicated and capable executive management team of full-time employees. A full-time in-house executive team will ensure that c-level officers are dedicated to the NSTC's mission and will reduce potential conflicts of interest that stem from holding leadership roles in multiple organizations. The CEO will lead the executive management team and oversee day-to-day operations and execution of strategy, as well as report to the board and deliver on the NSTC's overall success metrics. The CEO should strive to engage the semiconductor ecosystem while fostering a culture of diversity, equity, and inclusion. The CEO's management team should include:

- **Chief Technology Officer** – Oversees technology strategy, roadmapping, and program management
- **Semiconductor Chief Operating Officer** – Oversees the coordination of work at semiconductor execution facilities and aligns NSTC program needs with capabilities across the NSTC network
- **Packaging Chief Operating Officer** – Oversees the coordination of work at advanced packaging execution facilities, acts as general manager for the NAPMP, and aligns with capabilities across the NSTC network
- **Chief Investment Officer** – Oversees the NSTC's investment fund
- **Chief Talent Officer** – Oversees NSTC talent as well as workforce development programs and coordinates efforts throughout the ecosystem
- **Chief Defense Business Officer** – Oversees defense-related projects and acts as liaison to the Microelectronics Commons
- **Chief Administration Officer** – Oversees marketing and communications, legal, intellectual property, contracts, human resources, security, and IT
- **Chief Financial Officer** – Oversees finances, accounting, risk, and compliance

The NSTC must have the tools to attract the top talent required to fill these executive positions. These roles must be filled as quickly as possible as the NSTC is founded. One area that deserves a strong emphasis from the outset is in establishing the NSTC brand through its marketing and communications team. In addition, roles such as technology transfer, customer satisfaction, international partnerships, and government relations will emerge and evolve as the entity grows its capability and should be managed as needs arise.

A suggested organizational chart is presented in **Figure 1**.

To be agile, the executive team must have the decision-making authority and budget approval control to keep pace with and operate at the speed of the semiconductor industry. In addition, the executive team should convene leadership from other related programs in an ongoing manner to ensure coordination across the CHIPS R&D programs.

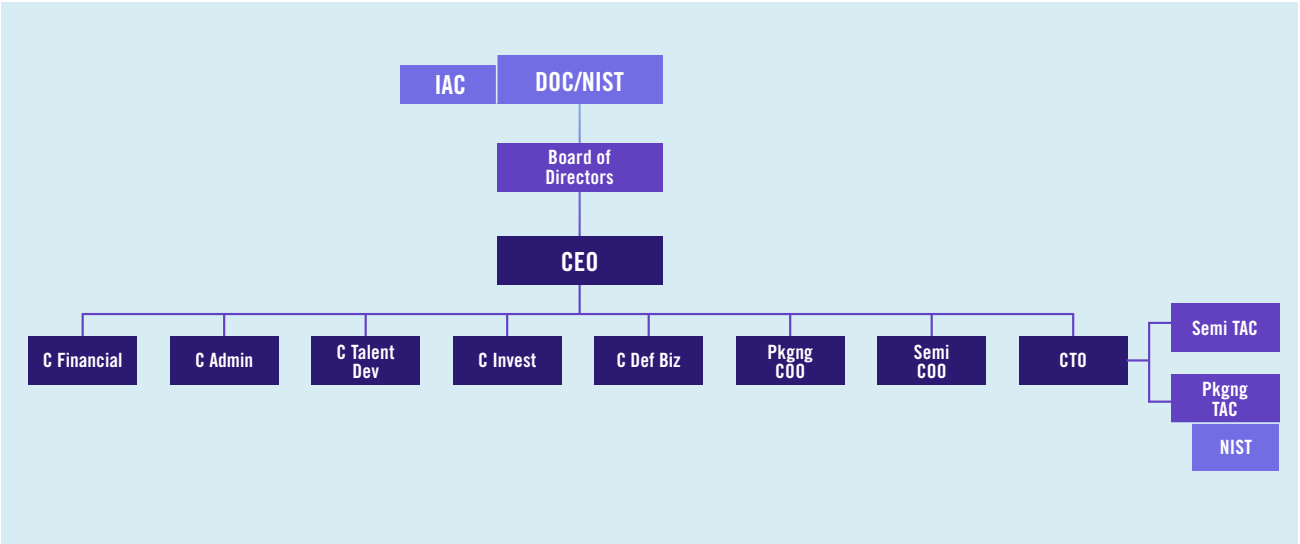


FIGURE 1. NSTC ORGANIZATION CHART WITH GOVERNANCE AND ADVISORY BODIES. THE NAPMP IS MANAGED BY THE PACKAGING COO AND THE PACKAGING TAC, ALONG WITH NIST.

Technical Advisory Committees

The NSTC will require technical expertise driven by market demands from across the ecosystem to ensure it pursues the most promising and impactful technology programs. The CEO should establish two technical advisory committees (TACs): one each for semiconductor fabrication and advanced packaging technologies, both comprised of external experts. The Packaging TAC should be responsible for developing and guiding the agenda and priorities of the NAPMP in close collaboration with NIST.

The TACs should be charged with making technology decisions that best align with the NSTC's and the NAPMP's strategy to provide the most benefit to the domestic ecosystem and align with the CHIPS R&D priorities and objectives. In addition, the TACs should provide input into the technology strategy, represent industry and academia's technical interests, and vet and prioritize breakthrough challenges. The TACs should review ongoing program progress and set guidelines and criteria for Go/No-Go decisions at critical milestones in a stage gate process.

Each TAC should consist of approximately 15 members with significant expertise in technology and product development. TAC members should have experience commensurate with a vice president level in industry. Individuals may either serve on the board of directors or a TAC, but not both simultaneously. To ensure that it inclusively reflects the ecosystem, each committee's composition should consist of representatives from the following:

- NSTC CTO
- 4-5 Integrated Circuit Manufacturers, Design Firms, and End System Makers
- 2-3 Semiconductor Equipment, Material, Electronic Design Automation, and IP providers
- 2-3 Universities
- 2 National Labs
- 2 DOD or Defense Industry
- 1 Startup Ecosystem (e.g., serial entrepreneur, entrepreneur-turned-investor)

Additional federal government representatives as deemed necessary by DOC/NIST, DOD, and DOE
The NSTC CEO has oversight over the performance of both TACs and is responsible for adding and removing TAC members. The NSTC CTO will co-chair the TACs alongside a nominated member of the TAC. The co-chairs are responsible for organizing the meetings and creating a cooperative and collaborative dynamic that leads to decisions that best benefit the NSTC and the ecosystem (rather than any specific entity or region). Members of the TAC, excluding the CTO, should serve staggered 2-year terms with an option for a 1-year reappointment to ensure continuity over ongoing programs, simultaneously providing a constant influx of new ideas, but staying consistent with the vision and long-term technical agenda.

Relevant technical directors at NIST and the DOD should participate on the TAC and have regular communications with the NSTC CTO to ensure alignment on R&D efforts across the CHIPS R&D programs as well as the DOD Microelectronics Commons.

There must be strong coordination and collaboration between the TACs to ensure the NSTC pursues and delivers on full-stack innovation. Strategies to foster this linkage include forming a joint sub-committee chartered with integrating scope and roadmaps, requiring multiple joint TAC meetings a year (especially when establishing goals), and collaborating on the long-term strategic direction.

The individuals who comprise the TAC must provide world-leading expertise in their domains to assist the NSTC in pursuing the most impactful technical programs. By placing the technology deliberations outside the board of directors, the NSTC can enhance neutrality by separating corporate and financial strategy from technology focus and decisions.

Staffing the NSTC to Achieve its Mission

Staff will be required, with the proper expertise, to carry out the daily operations of the NSTC commensurate with its annual budget, operations, and membership base. This staffing should primarily be focused on technical experts capable of directing, overseeing, and implementing the ambitious R&D and prototyping agenda of the NSTC, as well as workforce development and startup investment experts. Other roles include experts in legal and contractual matters including Other Transacion Authority, procurement, technology transfer, information technology, financial management, marketing and communications, and stakeholder management to ensure the success of the whole organization.

The NSTC must cultivate a team of experienced and capable technical staff that implements the day-to-day operations. This team should be direct hires that help the NSTC and TACs make sound technical decisions, serve as interfaces to the semiconductor and packaging community, guide startups, suggest innovative approaches to execution, and act as technical thought leaders.

An important part of the technical staff will be the NSTC's program managers, who will be critical to the success of the organization and delivering full-stack innovation through Breakthrough Challenges. These roles should report to the CTO and COOs and be responsible for helping to craft Breakthrough Challenges with the CTO and TACs, overseeing the solicitation and management of those programs with the COOs, and guiding entities such as startups through the NSTC's available services. One important aspect of the program managers' responsibilities is to monitor and facilitate work

conducted by non-NSTC personnel at industry, academic, and national laboratory facilities. The program managers will provide coordination of efforts across multiple parties and management of timelines and resources while also ensuring that the program objectives are still relevant and on track, therefore serving as the vital intermediary between the NSTC and the facilities where work is executed. A primary role of COOs will be to form a network of hubs with NSTC participants and coordinate cross-hub program management and effective interactions across hubs.

As is common in microelectronics public-private partnerships, the NSTC should host assignees from industry and academia to foster collaboration and cross fertilization of ideas. At steady state operation of the NSTC, the staffing mixture might consist of 70% NSTC employees and a dynamic influx of 30% industry and academic assignees, a ratio comparable to SEMATECH in its early years. [7] This ratio provides a balance of preserving know-how while also infusing outside perspectives. The assignee program should be structured to incentivize companies to send their best and brightest to benefit their own company as well as their projects of interest at the NSTC.

Additionally, administrative staff have a vital role to ensure the NSTC stands as an organization on its own. Strong legal and IT departments will be important to the NSTC's success. The legal team at the NSTC will manage numerous contracts around intellectual property, facility access, procurement contracts, and a large consortium member base. During operations at the NSTC, proprietary and sensitive information about facilities will be generated that must be protected to maintain trust between the NSTC and the ecosystem. Leveraging ecosystem data through analysis could potentially provide leap-ahead capabilities that accelerate all other innovations. The IT department will be a lynchpin that secures data and builds a platform that allows member companies to view, analyze, and innovate within a trusted environment.

The total number of staff at the NSTC will be commensurate with its scope and agenda to maximize the impact for its members. The Semiconductor Industry Association recently released a report that details case studies on relating the annual budget to employee count for notable active semiconductor research organizations that operate both with and without fabs. [8] These examples can be used to ensure the NSTC is staffed efficiently to execute its mission.

In addition to full-time employees and assignees, the NSTC can be an accelerator for workforce development by funding post-doctoral fellowships, graduate students, undergraduates, as well as technician trainees and worker re-skilling courses. These positions will conduct work directly related to the NSTC's R&D agenda and operations, while simultaneously serving as valuable hands-on training opportunities. The following section describes the selection criteria for NSTC's Breakthrough Challenges, which include the impact on workforce and emphasize the integration of workforce development into the NSTC's agenda. These efforts will be pursued in coordination with other workforce development initiatives across the industry.

Foster Inclusivity with a Flexible Membership Model

A flexible membership model for the NSTC considers the diversity and capabilities of the ecosystem, encouraging members to participate in a way that best suits them. Bringing together hundreds of organizations representing industry, startups, academia, and national laboratories requires flexibility to meet the needs of each type of entity while maximizing the ability to collaborate, innovate, and deliver.

Given the complexity of this task, the Semiconductor Alliance developed the following guidelines for the NSTC as it structures its membership model:

- Lower the barrier for participation through a simple tiered membership model with a modest base fee and mechanisms for program-specific contributions
- Allow flexibility to satisfy the unique requirements of various stakeholders throughout the value chain so that value can be extracted depending on need
- Incentivize cooperation between members to allow full stack innovation and market shaping goals that are only possible through collaboration
- Create a system of reciprocity and complementarity with U.S. government funded programs such as Microelectronic Commons and Manufacturing USA Institutes
- Establish rules of engagement for intellectual property ownership and sharing

Intellectual Property Recommendations*

The NSTC must manage the complex issues surrounding Intellectual Property (IP). This includes establishing a pre-negotiated IP framework that creates up-front expectations and incentives for participants to contribute IP, accomplishes an ambitious technical agenda, fosters collaboration, and protects inventor rights. The following recommendations are a set of high-level IP considerations to guide the incubation of the NSTC. These recommendations come from researching the models of similar organizations in the field of microelectronics, as well as public-private partnerships in other fields. [5; 7; 9] As mentioned above, the NSTC must establish a dedicated team under the Chief Administration Officer responsible for legal and IP to manage and update the IP framework as the NSTC's needs evolve.

The NSTC will require comprehensive participation from its participants, including the managed contribution of their relevant IP, to ensure collaboration and acceleration of R&D. The NSTC should implement a multivendor and network-wide platform of software and hardware capabilities that enables the execution of its technical agenda. This platform should accommodate solutions for Electronic Design Automation (EDA) tools, IP design blocks, Process Design Kits (PDKs), cloud tools, physical tools, baseline flows, test methodologies, and other IP. This platform can also assist participants from all parts of the ecosystem to commercialize innovation. While general guidelines will align IP with national interests and long-term value creation for the NSTC and its participants, specific terms should be negotiated upfront prior to each major work program, allowing for situation-specific handling of program participants while balancing the need to commence work expeditiously. All NSTC IP must be subject to export control laws and regulations, including the International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR).

Navigating issues around participant-contributed IP (i.e., background IP) and newly developed IP (i.e., foreground IP) prior to the commencement of work is critical to maximizing expectations, participation, and opportunities to transition technology from NSTC programs to universities and private industry. The NSTC should create clear expectations of participation and use of research outputs. Specifics relating to background and foreground IP are discussed below.

*This Framework and the content of this paper do not qualify as legal advice. Readers are encouraged to consult with counsel regarding rights and responsibilities with respect to the content herein.

Background IP Considerations

The NSTC must protect background IP to encourage wide collaboration and to incentivize its use for NSTC research. As an example, protections could include paid-up licenses only for NSTC use and field of use restrictions for a third-party participant's use beyond NSTC research. The background IP contributor should commit to making the technology available under fair, reasonable, and non-discriminatory (FRAND) terms. If terms are not acceptable to the NSTC or the contributing entity, the participant should not disclose or contribute background IP for R&D programs. Such sharing of background IP will help widen its usage and be an avenue for foundries, OSATs, and other inventors to expand their research program and, in turn, their customer base.

The NSTC could encourage participants to offer their respective background IP to the NSTC and indirectly to other NSTC participants by:

- Pre-negotiating royalty fees (if any) for use of any contributed background IP that becomes part of foreground IP in a commercial device.
- Pre-negotiating the right of the background IP contributor to use any resulting foreground IP.
- Acting as a neutral arbiter in certain IP negotiations among NSTC participants and users.
- Establishing a standard NDA that all participants subscribe to which protects parties from the disclosure of non-public information.

Foreground IP Considerations

Foreground IP is based on research that the NSTC, its members, or its users fund. Foreground IP could result from background IP that individual organizations contribute. Ownership rights of foreground IP should derive from the active participation in the research, i.e., inventorship.

The NSTC R&D that results in foreground IP could occur in at least three scenarios (described below). It should have established methodologies for handling IP in these scenarios.[7]

1. Common projects where all NSTC participants contribute and receive a license to use resulting IP for research and commercial use
2. Program-specific projects, where only a subset of NSTC participants and funders for a specific R&D project participate and receive ownership or licensing rights, depending on the level and type of contribution
3. Custom projects where an organization pays the NSTC to conduct the organization's own research, and that entity retains ownership of the resulting IP

Foreground IP generated with NSTC funding should be made available to participants for R&D purposes through pre-negotiated and paid licenses. For commercial usage, the pre-negotiated royalty structure should incentivize the manufacturing of technology within the U.S. and provide an additional NSTC revenue stream. The NSTC must develop a set of criteria to emphasize usage in U.S. manufacturing where possible. Participants who wish to join an ongoing program after its inception, or wish to make use of IP already created, may pay royalties or a "catch-up" fee to leverage or access the IP. At the same time, if an organization uses IP that results from NSTC research outside the U.S., a royalty fee should be imposed to encourage reinvestment in U.S. manufacturing, research, and development

Patent Considerations

The NSTC should establish a set of protocols that dictate when patents can be filed, which organization files the patents, and which organization is responsible for the legal, filing, and ongoing patent maintenance fees. NSTC committee review boards

and protocols could guide decisions on whether to patent, publish, or protect IP as trade secrets. All publications should align with a set of established protocols that prevent inadvertent loss or dilution of IP or know-how. When publications are approved, the publication thesis or content should emphasize the "why the results are important" and "what the research accomplished" as opposed to the "methodology" of the discovery. This would preserve the valuable know-how for NSTC participants while accelerating public participation in semiconductor research.

The NSTC should act as a channel partner for participants to encourage collaboration and aggregation of disparate sources of IP into valuable market solutions that financially benefit all parties involved. Establishing this culture of open contribution, innovation, and IP protection will ensure the nation's best capabilities are brought to bear on problems that no entity can solve on its own.

Defining and Measuring Success for the NSTC

In order to stand the test of time, the NSTC must ensure that its stakeholders derive measurable value from their participation in the NSTC, while also conveying that its mission is much greater than the sum of its participants' interests. The NSTC has a responsibility to the nation to show that American innovation can translate into American growth – that there are clear pathways to transition revolutionary technologies from lab to fab, domestically – and that the U.S. has secure access to the technologies it needs to defend its national and economic security. The NSTC will also be responsible for fostering a flourishing startup ecosystem within the U.S. and for helping to build the robust semiconductor workforce of the future. An important step toward achieving these objectives is to define what it tactically means to succeed with respect to each of them and how to measure that success, so that NSTC leadership can be held accountable.

Core values are the north star that ensures the NSTC remains committed to its mission. We propose the following core values:

- **Neutrality** – align and prioritize whole-of-nation objectives
- **National Impact** – strive for improving national and economic security
- **Inclusivity** –diversify the NSTC's membership across the ecosystem
- **Technology Disruption** – accelerate technology roadmaps; catalyze startups
- **Talent** – grow semiconductor talent base

Within the context of these core values, the DOC should set the objectives for the NSTC's board of directors that are tied to, and aligned with, the overarching national goals for the NSTC. To ensure that NSTC leadership is held accountable to the nation to fulfill the NSTC's mission, the board of directors should establish both a measurable set of objectives and corresponding metrics for the NSTC leadership. The executive team should utilize frameworks, such as better business scorecards or "objectives and key results" (OKRs), to holistically evaluate the NSTC's performance against its metrics at all levels of the organization on a regular basis. In the Appendix, we provide more detailed recommendations for how the DOC and NSTC leadership can set appropriate metrics for various levels of the organization.

The NSTC is an unprecedented opportunity to create an enduring national resource that establishes U.S. leadership for decades to come. The NSTC should foster full-stack innovation while also providing access to resources that lower barriers for innovation to overcome the manufacturing "valley of death". Dynamic and fair governance is critical for the success of such a catalytic, collaborative, and whole-of-nation endeavor. Establishing an organization that

becomes a neutral, coordinating focal point for the ecosystem with a reliable set of full-stack prototyping capabilities will accelerate the commercialization of technologies from lab to fab. Embracing the core principles of governance outlined above – neutral, agile, experienced, evolving, and inclusive – along with a well-coordinated programmatic effort overseeing a network of existing and future infrastructural facilities across the nation will be critical to successfully implementing the NSTC.

Setting an Ambitious, High-Impact Technology Agenda

To achieve its mission and to stand the test of time, the NSTC must be a powerful engine for translating American innovation into American growth. That is, it will need to facilitate the development of revolutionary, market-shaping technologies and shepherd them from "lab to fab" domestically.

In the paper, *American Innovation, American Growth: A Vision for the National Semiconductor Technology Center*, we identified two primary difficulties that currently limit the U.S. semiconductor ecosystem's ability to translate its world-leading R&D into market-ready technologies domestically:

- The Complexity of Pursuing "Full-Stack" Innovation
- The Difficulty of Bridging the "Valley of Death"

In order for the NSTC to increase the U.S. ecosystem's ability to translate American innovation into American growth, it needs to set ambitious, high-impact technology agendas that address both of these difficulties while nurturing unexpected sources of innovation. To that end, we proposed that the NSTC focus its technology funding on creating and executing Breakthrough Challenges. We envision a Breakthrough Challenge as a technologically disruptive program that:

- Has various applications of substantial importance to the U.S. economy and national security;
- Focuses on what will be the industry state-of-the-art in the medium to long term; and
- Addresses problems that no one company or organization can solve on its own – that is, efforts that require collaboration across organizations.[5]

Well-defined, effectively managed Breakthrough Challenges will address the issue of full-stack innovation by uniting the best innovators from around the country to work together to develop revolutionary new technologies with substantial market impact. Through a Breakthrough Challenge program, the NSTC will be able to provide funding and resources to a variety of relevant projects, led by teams of participants, that address various aspects of the stack in different ways. By supporting a diverse portfolio of projects and building connections between them, the NSTC will maximize its chances of generating "winning" next-generation technologies that successfully transition to market. Effective Breakthrough Challenges will address the manufacturing valley of death problem by providing funding to enable prototyping and scaling of promising technologies, as well as by connecting innovators with the facilities, tools, resources, and collaborators they need.

Because Breakthrough Challenges will form the core of the NSTC's technical agendas – and, consequently, will be critical to the realization of the NSTC's mission – it is of utmost importance that the NSTC have a robust set of frameworks, criteria, repeatable processes, and experts that it can leverage to shape them. In this section, we explain how the NSTC should select its Breakthrough Challenges to ensure that they are revolutionary, high-impact programs that effectively address the dual challenges of pursuing full-stack innovation and bridging the valley of death.

Determining Proper Scope for Breakthrough Challenges

In order to be high-impact, Breakthrough Challenges need to focus on driving revolutionary, full-stack solutions to pressing market problems. They must strike an appropriate balance between being ambitious and broad enough to impact societal challenges, while also being actionable and measurable against success metrics. Furthermore, the NSTC must be able to communicate how Breakthrough Challenges can create impact in the existing landscape of R&D needs. The following hierarchy of challenges can act as a frame of reference to help the NSTC scope and communicate its Breakthrough Challenges. This hierarchy is not meant to be prescriptive, but rather a tool to help simplify the difficult process of identification and communication:

- **Societal Challenges** – Broad, society- and civilization-wide challenges that, if solved, improve the quality of life for the world's population. Examples include combating climate change, improving healthcare, and reducing global energy consumption. The NSTC should be able to articulate how its Breakthrough Challenges will advance efforts to address societal challenges; this will aid the NSTC in communicating the relevance and impact of its work to the government and to the public.
- **Grand Challenges**† – Challenges facing the development of technology that, if solved, can unlock new markets and promote U.S. national security. These are broad technology challenges related to applications and use-cases for semiconductors, e.g., information and communication technologies, defense, healthcare, etc. Grand Challenge examples include the need to increase the energy efficiency of computing to avoid outstripping global energy production (highlighted as one the Semiconductor Research Corporation's Decadal Plan's "Five Seismic Shifts") and the challenge of advancing computing into the zettascale era (highlighted in the President's Council of Advisors on Science and Technology's (PCAST) 2022 report, "Revitalizing the U.S. Semiconductor Ecosystem"). [10; 11] Grand Challenges impact our ability to address Societal Challenges, but they are defined too broadly to drive focused, measurable NSTC work programs.
- **Breakthrough Challenges** – Specific, measurable, and actionable challenges that have a clear connection to important Grand Challenges and that, if solved, could ultimately move the needle on Societal Challenges. The NSTC will address these Breakthrough Challenges through its R&D and prototyping efforts. Examples of these Breakthrough Challenges include realizing 100x power reduction in data center applications and establishing a chiplet platform for use in heterogeneous integration. While each Breakthrough Challenge should be specific and measurable, it still should be written broadly enough to allow for competition of ideas and a variety of technical approaches and innovations across the stack. In other words, it should be possible to partition the Breakthrough Challenge into constitutive Actionable Problem Statements – i.e., specific component objectives that cover various current shortfalls and opportunities for innovation across a part or multiple parts of the stack. When the NSTC issues a call for proposals from participants for competitively selected projects that address multiple paths to Breakthrough Challenges, it should frame that call around Actionable Problem Statements. Using Actionable Problem Statements to frame calls for proposals will help both participants submitting project proposals and the NSTC to ensure that proposed projects are within scope; it will also help the NSTC ensure that it selects a diverse range of projects that address the full stack.

† This definition of "Grand Challenge" is the same as that used by PCAST and the Industrial Advisory Committee.

Figure 2 provides an illustrative example of how the NSTC draws connections between a Societal Challenge, a Grand Challenge, and a high-impact Breakthrough Challenge with constitutive Actionable Problem Statements that it could use to issue a call for project proposals.

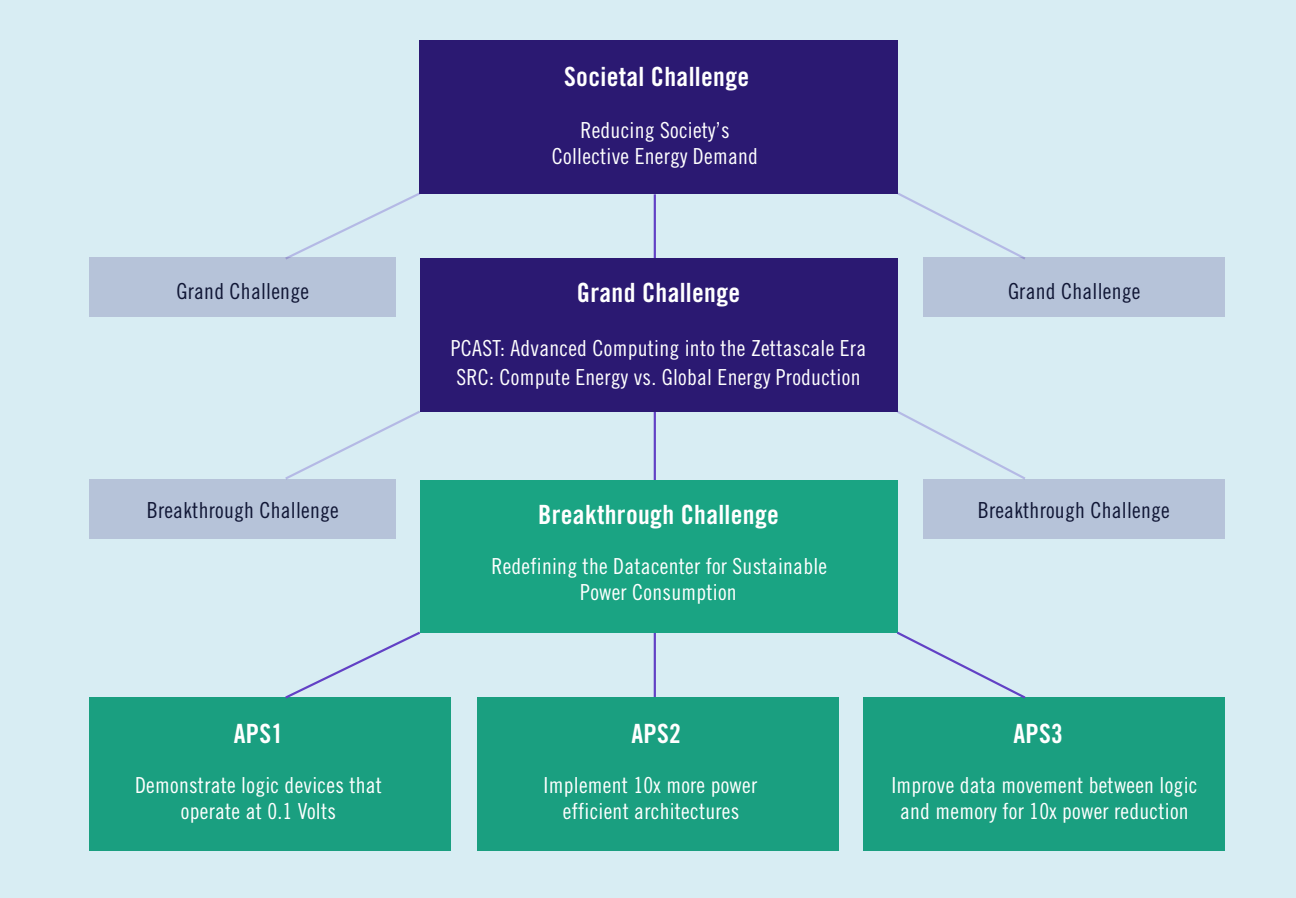


FIGURE 2: EXAMPLE BREAKTHROUGH CHALLENGE AND ACTIONABLE PROBLEM STATEMENTS (APS) ALIGNED TO A GRAND AND SOCIETAL CHALLENGE.

Identifying, Evaluating & Prioritizing Breakthrough Challenges

The CHIPS Act specifies that the NSTC's technical focus areas should include advanced semiconductor manufacturing, design and packaging research, and prototyping that strengthens the entire domestic ecosystem. [12] However, it appears to leave decisions as to how that guidance should translate into particular work programs to the discretion of the NSTC's leadership. Here, we recommend an approach for how the NSTC can identify, evaluate, and prioritize Breakthrough Challenges.

While the NSTC's TACs will be responsible for identifying, evaluating, and prioritizing potential Breakthrough Challenges, they will need ongoing support in surveying the ecosystem, staying abreast of industry roadmaps and strategies, and studying market needs. To that end, the NSTC should form a dedicated team of subject matter experts with strong knowledge of market trends and future technology needs whose role is to provide information and recommendations to the TACs to inform the Breakthrough Challenge selection process. These subject matter experts will play an active role in the ecosystem. They will participate in industry working groups and roadmapping efforts, convene experts from all segments of the ecosystem for NSTC workshops (designed to help narrow Grand Challenges into Breakthrough Challenges), and work with industry to identify high-impact market challenges and opportunities. This team of NSTC subject matter experts will distill findings and recommendations to present to the TACs on a regular basis, so that the TACs have robust, well-supported lists of potential Breakthrough Challenges to evaluate. Figure 3 illustrates the various factors this team will consider when presenting potential Breakthrough Challenges to the TACs.

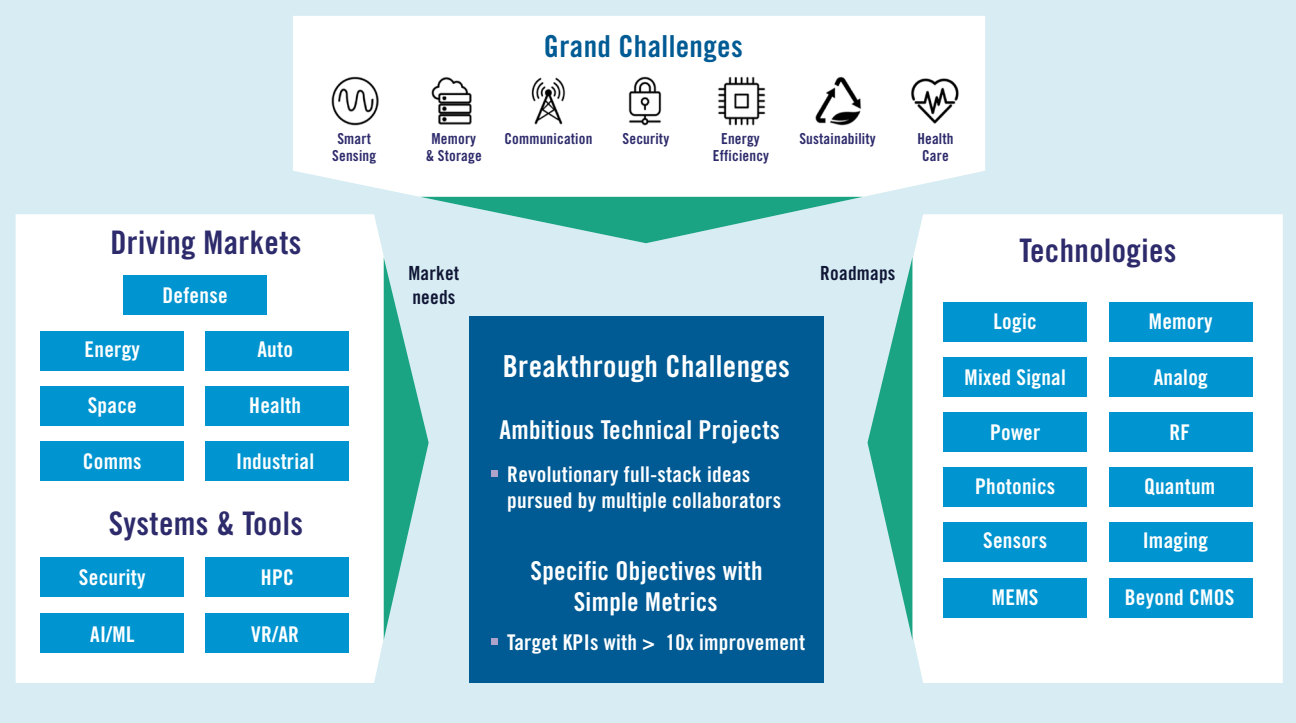


FIGURE 3: FACTORS SHAPING POTENTIAL BREAKTHROUGH CHALLENGES

Once the NSTC's TACs have a shortlist of potential Breakthrough Challenges, they should use a standard scorecard both to evaluate and, if necessary, prioritize them. The criteria in the scorecard should be designed to ensure that selected Breakthrough Challenges are revolutionary, with line of sight to solutions, broadly useful to the ecosystem, aligned to market needs, within NSTC's scope, and likely to be manufacturable with the potential for a sound business case. **Figure 4** shows our proposed Breakthrough Challenge Scorecard, which includes detailed questions that the TACs can use to assign point ratings for each category.

The criteria and corresponding questions in this scorecard are also applicable to the NAPMP's technical programs. Both TACs (the Semiconductor TAC and the Packaging TAC) should leverage the same scorecard to ensure that the whole organization has a shared language and mindset for shaping, vetting, and prioritizing various aspects of its overall technical agenda. Ideally, many Breakthrough Challenges will require input and guidance from both TACs as they take full-stack approaches to technical challenges; this will make a shared scorecard even more valuable.

Category	Detailed Questions
Revolutionary Idea	• Is the program revolutionary; does it provide a significant improvement? • Does the program embrace innovation across the stack? • What is the economic and/or national security impact?
Achievability	• Is there line of sight to a solution, or is it too "blue sky"? • Is the TRL and MRL progression reasonable given the time frame?
Broad Usefulness	• Will the program benefit multiple participants in the value chain? • How well does the program engage the NSTC's stakeholders? • Will the program have a positive impact on the workforce?
Within NSTC's Scope	• Does the program address the need to improve US semiconductor or package manufacturing and/or address strategic imperatives? • Does the program benefit the domestic supply chain security? • To what extent are new capabilities required to implement the program?
Path to Manufacturing	• Can a path to manufacturing be articulated? Have risks been identified? • What level of interest in the program is there from manufacturer(s) and other value chain participants?
Cost Effectiveness	• Do the program's benefits outweigh the cost? • What is the estimated collective return on investment? • Are government and industry contributions leveraged effectively?

FIGURE 3: BREAKTHROUGH CHALLENGE SCORECARD

By leveraging these robust sets of experts, frameworks, criteria, and repeatable processes for shaping Breakthrough Challenges, the NSTC will be able to distill the most pressing market and technological challenges of the coming decades into compelling, galvanizing Breakthrough Challenge programs that will propel U.S. innovation and leadership. Moreover, the NSTC will be able to bring the full range of the U.S. ecosystem's strengths to bear on these programs, innovating across the full-stack to create manufacturable, market-shaping technologies with profound, lasting impact.

Creating a Robust Network and Operating Model for Executing the Technical Agenda

The long-term success of the NSTC depends not only on its ability to set an ambitious, high-impact technology agenda, but also on its ability to execute those agendas effectively and efficiently. There are three keys to ensuring that the NSTC effectively and efficiently delivers on its mission.

First, the NSTC needs to start strong by strategically assembling and leveraging a network of diverse, existing facilities and capabilities it can use immediately to begin making progress on its technical objectives. If the U.S. were to wait for entirely new facilities to be built to commence the NSTC's work, we would risk falling behind in the race for global semiconductor leadership.

Second, once the NSTC is operational, it needs to continue to fuel innovation and technology commercialization by investing regularly in new "enabling capabilities" that support ever evolving and more advanced work, staying ahead of market trends, and enhancing the NSTC's value proposition to its participants and to the nation. Examples of such enabling capabilities include test structures, baseline flows, design tools, modeling and simulation tools, characterization tools, etc. In addition to investing in enabling capabilities, the NSTC will also need to make investments in filling infrastructural gaps that hold back innovation.

Finally, the NSTC needs world-class program management to ensure that it utilizes its resources to maximum advantage, effectively orchestrates its complex projects, and drives teamwork across diverse programs and organizations as the focal point of the U.S. semiconductor ecosystem. The following subsections explain how the NSTC can put these three keys into action.

Leveraging a Network of Existing Facilities, Capabilities, and Strengths

Fortunately, many of the resources that the NSTC and its participants will need to get started already exist. However, today, they are not widely accessible, catalogued in a comprehensive and accessible way, or stitched together with an overarching program management layer. By addressing these gaps – in ways we will discuss in later subsections – the NSTC can make the most of the investments the U.S. ecosystem has already made, target its own investments strategically to fill existing gaps, and begin making impact quickly.

Strengthening the Case for a Network of Existing Resources

However, speed is not the only reason why the NSTC should begin by leveraging existing infrastructure, tools, and capabilities. Two other compelling reasons include: 1) having a diverse set of resources available, such that it is possible to provide projects with resources that are fit-for-purpose at different stages of technological development; and 2) leveraging clusters of special expertise and resources where they exist throughout the country. The following pages elaborate on these points in turn.

Ensuring the NSTC can Provide Projects with Fit-for-Purpose Resources

The technical requirements (i.e., the tools, infrastructure, processes, etc.) for demonstrating a new innovation in a single chip are vastly different from the requirements for producing a chip that can be manufactured at commercial scale. Generally

speaking, it is impossible to assess and to prove the suitability of a technology for high-volume manufacturing in a small R&D laboratory. It would be extremely cost-prohibitive and unacceptably risky to run an early demonstration of a small batch of chips on the exquisite, highly controlled lines found in commercial or near-commercial environments. If the NSTC is to help innovators to prototype and to scale their technologies to bridge the lab-to-fab divide, it will need to leverage a variety of facilities, tools, and resources that are suitable for various stages and types of technology development.

To begin parsing this challenge into requirements, it is helpful to define the different stages of technology development within the NSTC's scope and to characterize the types of capabilities relevant to each stage. The Semiconductor Alliance recommends that the NSTC measure the progress of innovations in terms of manufacturing readiness levels (MRLs), as the MRL scale considers not just technical readiness, but also manufacturability. Technology Readiness Levels (TRLs) must also be considered by the NSTC and aligned to its MRL scale. At a high-level, we propose that the NSTC and the NAPMP employ the following common set of stage definitions:

- **Proof of Concept:** Early demonstrations of a technology's feasibility, often demonstrated in R&D laboratories (e.g., university and national labs); usually MRL 1-3
- **Module Demonstrator:** This stage initially focuses on determining what other full-stack elements are necessary for the technology to achieve commercial success. Once gaps are identified and addressed, multiple technical elements are brought together to demonstrate the technology's benefit in a more complete system with manufacturing-relevant settings. These tend to be done in more advanced laboratory, prototyping, and low-volume production settings; usually MRL 4-6
- **Functional Prototype:** Multiple module demonstrators and other functional elements are brought together to create a prototype in manufacturing-relevant settings that precedes a ramp to commercial fabs; usually MRL 7-8

The NSTC should focus most of its efforts at the Module Demonstrator and Functional Prototype stages, but it must also be aware of and incubate promising technologies that are still within the Proof-of-Concept stage. **Figure 5** illustrates how the NSTC should map a diverse set of facilities, tools, and capabilities to projects across the technology development funnel.

By leveraging a diverse network of existing capabilities to satisfy the varied requirements of different projects, the NSTC will be equipped to execute its work both effectively and in a cost-efficient manner.

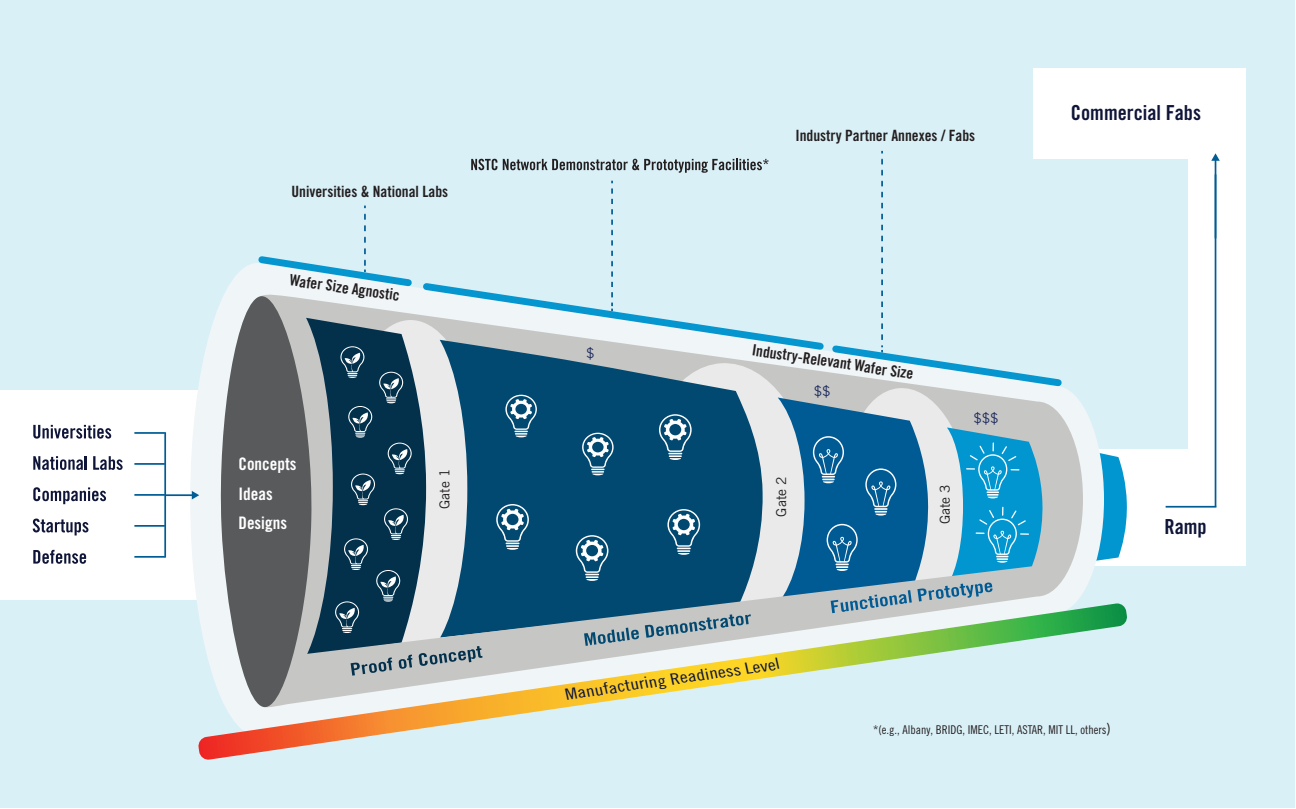


FIGURE 5: MAPPING RESOURCES TO TECHNOLOGY STAGES

Leveraging Clusters of Expertise & Resources Throughout the Country

There are several regions throughout the country that already have particularly high concentrations of production capacity; they support infrastructure, talent, and research activity in certain thematic areas or technology types. Rather than replicating what has taken decades and billions of dollars of investments to establish, the NSTC should incorporate these clusters of expertise and resources into its network.

In addition to these particularly notable centers of gravity in the U.S. ecosystem, there are also companies, universities, and national labs in other parts of the country that offer specialized – and, in some cases, unparalleled – expertise and capabilities in particular technical areas and use cases. Some, for example, meet the robust security and technical requirements for working on sensitive technologies for the DOD. **Figure 6** provides an illustrative snapshot of the number and broad geographic footprint of NSTC-relevant locations and capabilities in the U.S.

For the NSTC to serve the entire ecosystem – both private- and public-sector – and as a truly whole-of-nation effort, it must make effective use of relevant, valuable capabilities where they exist nationwide.

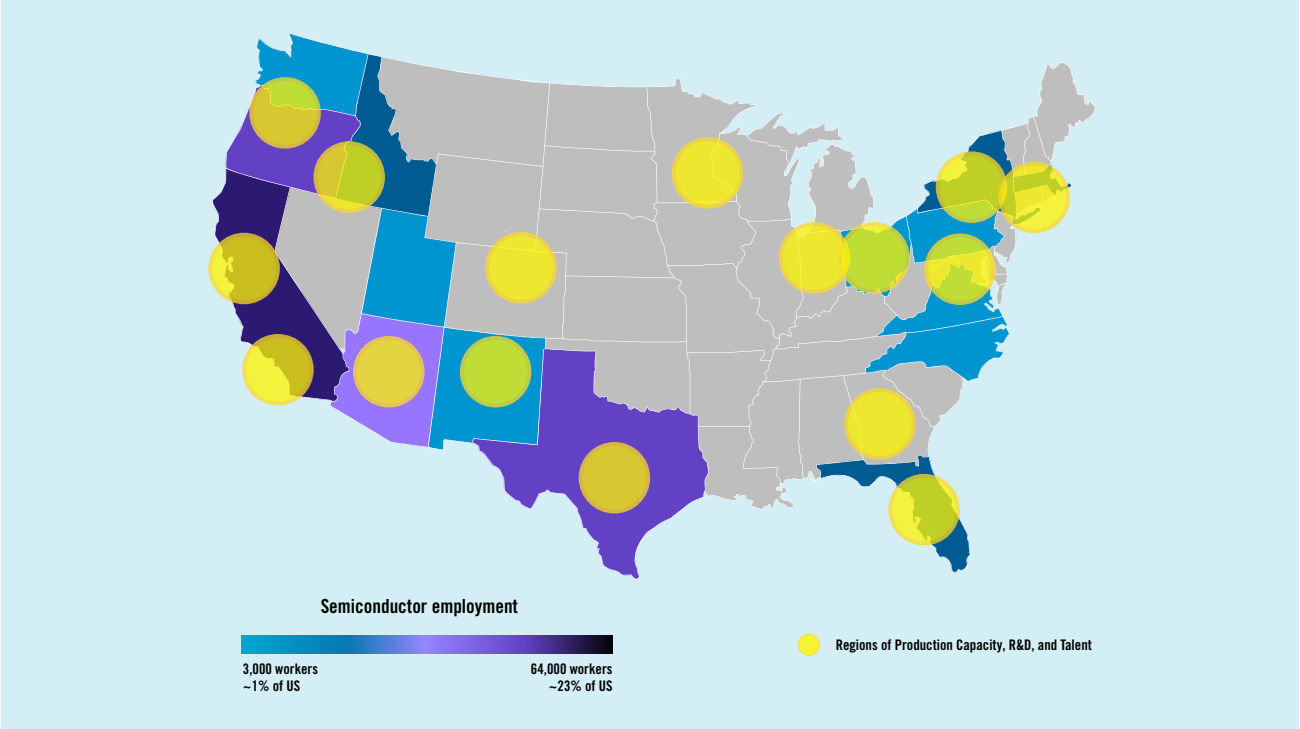


FIGURE 6: TALENT AND REGIONS OF STRENGTH IN THE U.S.[13]

Defining the Network

We propose that the NSTC's network comprise three core components: hubs, spokes, and annexes. It is important to note at the outset that these proposed network components and their corresponding definitions are not analogous to those proposed for the DOD Microelectronics Commons despite commonalities in terms (e.g., "hubs").

Hubs

There are already significant clusters of capacity, talent, and expertise in particular technology domains located in regions throughout the country. It is natural that these regions and facilities will become centers of gravity for NSTC activities. These centers of gravity will be logical locations for the NSTC to assign its program management staff for specific technology areas, as a substantial proportion of NSTC projects will likely pass through facilities in those regions at least once. Having program management sit in these locations – the convergence point for so many projects – will be advantageous for managing program logistics, as well as for fostering connections among projects and teams. Given that the semiconductor ecosystem is so capital-intensive and dependent on economies of scale, the NSTC should choose these centers of gravity to house many of the tools and other enabling capabilities it will invest in for the benefit of the ecosystem. Because these clusters of capacity, talent, and resources will play a such an important coordinating role in the execution of the NSTC's technical work, we call them **hubs**.

The term "hub" does not refer to a particular company, a particular entity's facility, or a specific region. Rather, it is a term for a concentration of program management, tools, resources, and capacity focused on a specific technology domain[‡]. Of course, centers of gravity that are selected to be "hubs" will, by definition, have at least one major R&D or commercial/production facility. For a hub to be successful, companies or other entities that own critical local facilities in the NSTC network will need to agree to provide access to relevant resources, personnel and enabling capabilities for the NSTC-defined technical programs. Additionally, NSTC staff at the hubs must be responsible for overall coordination of a Breakthrough Challenge program, which includes participation from multiple hubs, spokes, and annexes. For each Breakthrough Challenge, a hub should be designated as the lead coordinating body. The execution of the work at participant facilities will be conducted by those participants' staff.

To ensure a full-stack approach and the ability to support diverse projects, hubs should be focused on strengthening various semiconductor technology domains relevant to the value chain, e.g., system-design technology co-optimization, memory, logic, analog/RF/mixed signal, packaging. The NSTC should create hubs as necessary to execute its technical agenda and evolve them as the NSTC's priorities change. Hubs will need to cover cross-cutting elements of the stack like design, metrology and characterization, heterogeneous integration, and modelling and simulation. With continued investment, these hubs could become increasingly valuable centers of excellence in particular technical areas. They will always, however, be mutually dependent on each other and need to collaborate closely in order to succeed in developing full-stack, manufacturable technologies.

The NSTC CTO office, in conjunction with the TACs, will have the critical job of designing Breakthrough Challenge programs that leverage these diverse capabilities and encourage collaboration amongst teams working on projects throughout the entire NSTC network. The NSTC's program management will be responsible for ensuring that, when it comes

[‡] This concept of hubs is similar to the PCAST's idea of "coalitions of excellence", see reference 11.

to the execution of work, project teams consisting of the NSTC's participants avoid the pitfall of working in geographic and technology silos and, instead, work effectively across the stack and across the network of hubs.

Spokes

Many critical facilities, tools, and experts that are key to the execution of the NSTC's technical programs will be located outside of hubs. As **Figure 6** illustrates, relevant capabilities, talent, and resources exist throughout the country. These may include specialized facilities that focus on DOD needs, university laboratories with special expertise or capabilities in a particular area, or smaller commercial facilities. These facilities will play a critical role in carrying out technical projects, but they have smaller program management presence and are likely to have more targeted capacity and work volume than hubs. We call these locations spokes. Leveraging spokes will not only expand the NSTC's ability to execute work and enable it to take advantage of specialized capabilities throughout the country; this will also make it easier for the NSTC to catalyze and attract investment from states and regional entities across the country that seek to bolster their ability to contribute to the growing U.S. semiconductor ecosystem.

Annexes

For late-stage functional prototyping work, NSTC project teams will need access to commercial processing equipment, materials, and process flows. This work will take place in annexes, which are dedicated areas within or adjacent to semiconductor manufacturing facilities. In annexes, project teams will have access to the capabilities and resources necessary to refine their technologies and to demonstrate their potential for successful transition to commercial production. Potential annex-like facilities already exist today at locations in Arizona, Idaho, New York, and Texas. To the extent that the NSTC does invest in building new infrastructure in years to come, it should consider making some of those investments to leverage annexes to meet evolving needs.

By stitching together a network of infrastructure, tools, and resources that includes hubs, spokes, and annexes, the NSTC will create a powerful innovation engine capable of faster, more efficient, and more collaborative prototyping and scaling of revolutionary technologies than has heretofore been possible

Working with International Partners

When defining the NSTC's network of infrastructure, tools, and capabilities, it is important to remember that the U.S. semiconductor ecosystem already has robust and fruitful relationships with several prominent R&D partners, suppliers, manufacturers, and government semiconductor agencies in allied countries. Organizations like imec, CEA-Leti, Fraunhofer, A*STAR, ITRI, KAIST, and CIES have substantial capabilities and expertise, and are major drivers of global semiconductor innovation. It is important that the NSTC collaborate and cooperate with these like-minded entities to ensure successful delivery of programs and efficient utilization of resources. Establishing strong, long-term partnerships will contribute to diversity of thought, expedite access to missing capabilities, create a backup to critical and expensive capabilities, expand capacity, improve supply chain resilience, and lead to mutual success

Establishing the Network

While it is critical that the NSTC establish this comprehensive network of both domestic and allied

international facilities, tools, and capabilities, it is also a risky undertaking. As the NSTC's network grows, so will the costs and logistical challenges of managing it. The NSTC must be strategic and discerning as it identifies, vets, and onboards new hubs, spokes, annexes, and partners. To ensure that prospective new network elements provide a strong value-add to the NSTC, management should utilize a standard framework for evaluating candidates. To that end, MITRE Engenuity and the Semiconductor Alliance have developed a questionnaire that NSTC management can send to prospective hubs, spokes, annexes, and partners to determine whether they should be included in the NSTC network. **Figure 7** highlights some of the key considerations covered in the questionnaire.

MITRE Engenuity and The Semiconductor Alliance team have begun to collect and organize this facility data which can be developed into a platform that derives "flight paths" for Breakthrough Challenge program coordination. The NSTC should continue this work to help automate the coordination of work across facilities and different parts of the stack.

The NSTC should define and leverage a network of existing capabilities and provide input into Breakthrough Challenge selection to ensure some projects will successfully transition to industry within the first five years. With a whole-of-nation approach and the U.S. ecosystem's greatest strengths to support it, the NSTC will be a powerful force for translating American innovation into American growth and propelling the U.S. to global semiconductor leadership.

Facility Capability Considerations:

- Facility Fit and Expertise – technical and process alignment to NSTC program needs
- Technical Capability – technologies and expertise that can be deployed to programs
- Facility details – fab/lab space, class of clean rooms, office space
- Equipment/process/technology capability details – specifics on accessible technologies, including hardware and software tools
- Dedicated or available skilled technicians, operators, and engineers – resources that could be deployed to NSTC programs

Facility Operation and Execution Considerations:

- Accessibility, Capacity and Utilization – ability for the NSTC to access facility with personnel and utilize equipment for technical programs
- Cost Structure – details on the costs associated with accessing and utilizing capabilities
- Facility Operation – Program execution, decision making and prioritization
- Facility Augmentation or process flexibility – procedures for adapting existing capabilities and infrastructure
- Facility Access to external resources – ability to access additional funding or support from local, regional, state entities including government
- Facility EH&S – procedures and programs in place to ensure safe working environment
- Facility IP & Legal Protections – IP policies and practices for NSTC engagement models
- Workforce Development History – experience and history of participation on WFD activities and programs

FIGURE 7: KEY CONSIDERATIONS FOR NSTC FACILITY QUESTIONNAIRE

Investing in New "Enabling Capabilities" to Stay Ahead of Market Needs

Once its network of facilities, tools, and capabilities is established and running, the NSTC must remain focused on continuing to fuel its innovation engine. The rapid pace of technological advancement in the semiconductor industry will require that the NSTC invest regularly in new "enabling capabilities" to support its ever-evolving work, stay ahead of the market, and enhance its value proposition to participants and to the nation.

The term "enabling capabilities" encompasses all of the technologies, tools, and materials required to execute the NSTC's and NAPMP's semiconductor and packaging R&D and prototyping. Examples include test structures, EDA tools, wafer and substrate process and handling tools, advanced materials, metrology methods and characterization tools, PDKs, new foundry concepts, etc.

As the NSTC embarks upon its Breakthrough Challenge work, it will inevitably discover gaps in the enabling capabilities that exist within its network. As the focal point and key enabler of the U.S. ecosystem, the NSTC will have a responsibility to fill gaps that materially impact its ability to execute its mission. However, investment in enabling capabilities should not be purely opportunistic. It is of the utmost importance that the NSTC strategically plan its investments in enabling capabilities to ensure that they create maximum benefit for its work, while also increasing the value that the NSTC and its participants derive from that work. For example, investing in the ability to capture key data from wafer runs on baseline flows could yield near-term benefits for projects, but it could also enable the NSTC to create digital twins and simulation models that would become even more valuable with time, yielding great benefits for all future work.

Investment in enabling capabilities will be especially critical with respect to packaging. NAPMP funding should be deployed to build, equip, and operate facilities that perform advanced packaging R&D and prototyping. These investments will result in a more competitive domestic advanced packaging manufacturing ecosystem. The NAPMP will need to determine which technology building blocks to invest in to allow the domestic ecosystem to 1) ramp R&D to manufacturing and 2) enable technically differentiated products to be manufactured in the U.S. At a high level, these building blocks should be organized around three types of packaging workflows: a unit-level workflow, a wafer-level packaging workflow, and a panel-level packaging workflow. NAPMP investment should also create common cross-cutting capabilities that include test structures, standards, a chiplet library, new test capabilities, thermal management materials, metrology and characterization, and manufacturing process and equipment improvements that could be deployed to each of these three packaging workflows. The NSTC will need to make extensive use of the capabilities established with NAPMP funding to execute its own packaging R&D programs and projects. Because NAPMP-funded capabilities will be so critical to both NAPMP and NSTC technical programs, the NSTC and the NAPMP should have a common governance structure that makes it possible to optimize investments.

By investing regularly in high impact enabling capabilities, the NSTC will ensure that the value and strength of its network is much greater than the sum of its parts. These investments will also provide a steady buildup of capabilities at hubs, spokes, and annexes that strengthens the ability to execute Breakthrough Challenges and improves accessibility to participants. This will enable the NSTC to continue focusing on revolutionary, market-shaping technologies and on maintaining the long-term commitment and continued investment of its stakeholders. By providing unique and growing value

to participants, the NSTC will be able to fortify its business model by expanding the number of custom projects at the NSTC – a strategy that existing organizations like imec have employed with great success.

The NSTC's enabling capabilities and the opportunity to leverage them for custom projects will be valuable to organizations of all sizes, but especially to startups. Often, startups are hamstrung by their inability to access specific process flows, test structures, metrology tools, and manufacturing equipment to test and to validate their innovative technology. By helping companies to locate and to access the tools and capabilities that they need to advance their work, the NSTC can reduce barriers to bringing disruptive technology to market. Lack of funding is also a major barrier that startups face when seeking to access tools and capabilities, even when it is clear where and how to find them. The NSTC's investment fund can address this challenge by making "in-kind" investments in startups – that is, by covering the cost for startups to access critical tools and capabilities in exchange for equity.

An ever-evolving set of enabling capabilities housed throughout the NSTC's network will also be a valuable resource for the NSTC's workforce development programs. When students come to the NSTC for internships, fellowships, or post-graduate programs, they will be able to work on cutting-edge tools and flows with which they otherwise would have limited to no experience or exposure. This – along with the discussion of how the investment fund and enabling capabilities can lower barriers for startups – are critical examples of how keeping all of the NSTC's core functions (i.e., technical program execution, venture capital investment, and workforce development) under one organization, rather than distributing them across multiple entities, will allow the NSTC to maximize the value it creates for its stakeholders. Sustained, strategic investment in high impact enabling capabilities will be a driving force in making the NSTC an enduring national resource for decades to come.

Developing World-Class Program Management

Finally – but crucially – the NSTC needs world-class program management to ensure that it utilizes its network, enabling capabilities, and other resources to maximum advantage. The challenges facing the NSTC's program management team will range from project-level (i.e., how to coordinate substantial, complex technical projects across a large and evolving network) to the ecosystem-level (i.e., how to ensure that the NSTC serves as the focal point of the U.S. semiconductor ecosystem, driving collaboration and full-stack approaches across a wide range of related programs and entities). Successfully addressing these challenges and effectively executing the NSTC's technical mission will require both highly skilled individuals (including subject matter experts) to fill program management roles, as well a robust set of management tools, communication channels, and norms. This sub-section identifies the key functions of the NSTC's program management and outlines the critical success factors for each.

Once a Breakthrough Challenge has been identified and prioritized by the TACs and CTO, the NSTC's program management team's three key functions will be: 1) managing the call for project proposals and project selection; 2) coordinating projects executed at multiple participating facilities and their staff; and 3) ensuring coordinated, collaborative, full-stack approaches to innovation both across both the NSTC's projects and across the U.S. semiconductor ecosystem. These are discussed below.

Managing Overall Program Performance & Execution

In addition to being responsible for managing the process of selecting projects under Breakthrough Challenges, NSTC program management will be responsible for managing accountability to overall program performance across hubs. While one of the NSTC's main purposes will be to shepherd American innovations through the "valley of death" so that they can drive American growth, not all innovations can, or should, make it across that valley. Many technologies and approaches developed through Breakthrough Challenge projects may show promise early on, but later run into substantial challenges that limit their technical and market viability. The NSTC's program management will manage the stage gate review process and update the TACs during major milestone reviews to determine Go/No-Go decisions. The NSTC's program management leaders will closely interact with the execution teams and, consequently, will be able to provide informed analysis, insights, and recommendations to the TACs. In this capacity, the program management team will be critical to ensuring that the NSTC directs and prioritizes its funding and efforts in ways that are efficient, enduring, and likely to create high impact.

Orchestrating the Logistics of Individual Projects

In addition to coordinating the management and evaluation of Breakthrough Challenge programs through stage gates, the NSTC's program management leaders will be responsible for ensuring the effective orchestration across the hubs, spokes, and annexes for Breakthrough Challenge program delivery. To carry out this management role for the large, complex, highly distributed projects that the NSTC will undertake through BTCs, program management leaders will need:

A Robust Database of Network Capabilities

The NSTC's program management will need a structured, searchable, and up-to-date database solution that captures all relevant network capabilities. Since a database for capturing up to date domestic semiconductor manufacturing facilities and operations does not currently exist, it must be built for the NSTC. Initially, the database should focus on cataloging the equipment and capabilities within each facility, so that the NSTC can identify the right set of facilities for a given project, considering topics such as accessibility and material contamination protocols. It should be continuously updated and vetted. Over time, the database and database management system will grow to include operations data, similar to the manufacturing execution system (MES) and enterprise resource planning (ERP) data used in manufacturing facilities. By combining this data across facilities, the NSTC will be able to apply big data, machine learning, and statistical methods to identify best practices and to help build overall domestic innovation and lab-to-fab translation speed and quality. A centralized data repository will also support the creation and evolution of digital twins, which can further improve the matching of resources to project needs and accelerate innovation.

In addition to enabling program managers to identify critical capabilities and resources for projects within their purview, the national database will also enable participating entities to locate specific capabilities throughout the network that they need to accelerate their own innovations. The database of capabilities outlined above along with other development tools could eventually evolve into a platform that leverages artificial intelligence and machine learning to accelerate learning cycles. This will be highly valuable for all participants, but it will especially reduce barriers to innovation for small companies, academics, and innovative startups.

Management System for Scheduling, Handling Protocols, and Performing Transfers

With wafers, substrates, chemicals, and materials constantly moving from facility to facility, the NSTC's program management will need a common framework and shared tool for communicating requirements; scheduling work, tool use, and transfers; and managing logistics. Ideally, the management tool should also include easily accessible information about new material introduction rules for different facilities and equipment; this will protect equipment and flows from being contaminated or compromised. Ideally, this tool will become the first "go-to" resource for engineers from industry, academia, and government who are looking for the particular tools and resources they need to execute their R&D and prototyping projects.

A Repository for Experimental Data

In order for the NSTC to operate its programs and projects efficiently, its program management teams need effective tools for capturing and sharing institutional knowledge and information about past work. The NSTC should have a searchable repository for experimental data from its projects so that knowledge is not lost as employees and assignees come and go over time. Such a tool would minimize duplication of work, while also maximizing institutional learning and the value of lessons-learned from all of its projects.

Equipped with these resources, the NSTC will have a truly world-class program and project management approach that it can use to manage the complex and dynamic assets of the hub, spoke, and annex system.

Driving Coordinated, Collaborative, Full-Stack Approaches to Innovation

In order for the NSTC to drive full-stack approaches to innovation, it will need to foster and facilitate coordinated, collaborative work across both its own project portfolio and the full U.S. ecosystem.

To make sure that Breakthrough Challenges drive full-stack innovation, the NSTC needs to work with other key entities in the ecosystem to shape them. The NSTC's CTO office and TACs should engage regularly with industry, government (e.g., DOD/DARPA, the Microelectronics Commons, DOE, Manufacturing USA Institutes, national labs, etc.), and academia to discuss emerging needs and priorities. Regular touchpoints like leadership meetings, working sessions, and conferences will be valuable for maintaining this consistent engagement. As the NSTC streamlines Breakthrough Challenges into Actionable Problem Statements, it should be mindful of where relevant work is already taking place in the ecosystem and ensure that it sets a proper scope for its own work.

Coordinated, collaborative approaches are critical at the project level as well. When evaluating project proposals to determine which should receive NSTC support, the NSTC – as the focal point of the U.S ecosystem – should coordinate with other government and industry entities (e.g., venture capital firms) that may be interested in co-funding projects or in making complementary investments. As the slate of projects under a given Breakthrough Challenge fills up, the NSTC should evaluate how well the selected projects collectively cover the stack and how well they complement each other. In cases where there are gaps and deficiencies, the NSTC should work with partners throughout the ecosystem

to solicit gap-filling proposals and to help these other entities identify areas of unmet need that may fit into their own complementary agendas. The NSTC should encourage project teams to leverage the diverse resources within and across hubs, as well as build connections between teams during project formation. Stage gate reviews will be critical opportunities for evaluating how well Breakthrough Challenge projects are working across the stack and where program management can steer project teams toward the resources that they need to right their course if their approach is too narrow.

As the focal point of the U.S. semiconductor ecosystem, the NSTC must ensure that the philosophy of full-stack innovation and a spirit of collaboration permeate its work at all levels – from the highest levels of strategy-setting to the most tactical levels of project execution. When it succeeds in doing this, the NSTC will be a powerful force-multiplier for the U.S. ecosystem writ large.

Ensuring Long-Term Financial Sustainability

To compete well in any marathon, contenders must plan carefully how they are going to expend their efforts, as well as when and how they are going to refuel. While the roughly $11 billion dollars appropriated for the NSTC, NAPMP, and related CHIPS Act efforts may seem like a large quantity of money, it could, in fact, run out quite quickly if spent injudiciously (e.g., spread thinly across too many efforts, fragmented into duplicative programs, concentrated on a few all-consuming projects, needlessly duplicating infrastructure etc.). Likewise, if the NSTC does not create sufficient value for all participants, such that it can diversify its income streams to include substantial private revenue streams and state/local resources, the work and impact of the NSTC and NAPMP will peter out after the NSTC fully deploys this CHIPS Act investment. In this section, we recommend various ways that the NSTC should diversify its income streams, as well as set reasonable expectations for the long-term investment the NSTC will need to be financially sustainable so that it can continue advancing U.S. leadership in semiconductors for decades to come.

Defining "Financial Sustainability"

The first step in creating a plan to ensure the NSTC's long-term financial sustainability is to define what it really means to be "financially sustainable." As the Department of Commerce wrote in its September 2022 paper, "A Strategy for the CHIPS for America Fund," federal funding is meant to be a catalyst for additional investment in the NSTC from all segments of the U.S. ecosystem:

"The funding provided by the CHIPS Act of 2022 for the NSTC should be viewed as seed capital. The Department envisions an organization that grows over time to be a significant force for advancing innovation in semiconductors and microelectronics, with substantial financial and programmatic support from companies, universities, investors, and other government agencies, including those at the state and local levels." [14]

It is important, however, that the federal government does not treat this as a one-and-done investment – this should not be a seed planted and merely observed from a distance. Rather, the government should approach the NSTC as a long-term commitment which will require further investment in the future. In addition to being a key factor in the NSTC's financial viability, continued government funding is critical to ensuring that, over time, key government stakeholders still have a seat at the table when it comes to shaping the NSTC's priorities. If the NSTC were to become entirely – or almost entirely – privately-funded, it would likely prioritize short-term market needs over its original long-term mission. States and regional entities might increase their investment, but, without the counterweight of federal funding and involvement to ensure the NSTC remains committed to a whole-of-nation approach, this could lead to factionalism within the NSTC and regionally-motivated – as opposed to strategic – decision-making and investment. Furthermore, if industry believes that the government is not committed to longer-term funding for and engagement in the NSTC, it will be less likely bring

to the table significant investments of its own. In order for the federal government to ensure that the NSTC serves the whole ecosystem (both private and public-sector), prioritizes its long-term mission, and continues to take a whole-of-nation approach to innovation, it needs to continue to invest in and to be engaged with the NSTC over the long term.

If the NSTC will always have some level of government funding, what, then, does it mean for the NSTC to become "financially sustainable?" Based on the above, the answer is not that it should become 100% independent of public funds, relying only on private-sector revenue. Indeed, no other peer organization in the semiconductor industry has done so. Rather, the NSTC must strike a balance between diversifying its revenue streams to build a strong financial underpinning from private-sector revenue by creating value for participants and continuing to leverage public investment strategically. Existing and highly successful organizations like imec in Belgium, Fraunhofer in Germany, and the Semiconductor Research Corporation (SRC) in the U.S. illustrate what such a balance might be: these organizations have achieved a ratio of earned revenue to public-sector funding roughly in the range of 70:30 to 80:20, with the exact ratios varying over time. [15; 16] It is important to note that these organizations have been in existence for decades – imec since 1984, Fraunhofer since 1949, and SRC since 1982 – and that it took decades for them to achieve these ratios. Imec has created a diverse set of revenue streams that include membership in Industrial Affiliation Programs, direct contract-based R&D engagements with companies, and a venture portfolio. Fraunhofer has grown a substantial contract research business that now accounts for the majority of its revenue. To do this, these organizations had to invest in a robust set of unique capabilities that provided enough value for companies, universities, and others to turn to them as go-to resources. They had to build relationships, trust, and strong reputations with key customers and partners to bring them to the table, to secure business and investment, and to demonstrate success that could inspire others to work with them as well. This does not happen overnight, and it does not happen without continued investment and evolution to keep up with the changing ecosystem and market trends. Using imec's trajectory (illustrated in **Figure 8**) as a reference, a rough estimate of the time it may take for NSTC to achieve a funding ratio of 70:30 is 15-20 years. The analogy between imec and the NSTC is not perfect – their starting assets, infrastructure, and focus areas along the MRL scale differ – and the NSTC's ability to track imec's trajectory depends on numerous factors, so it is best to consider this estimate a point of reference and general objective, rather than a formal prescription or management metric.

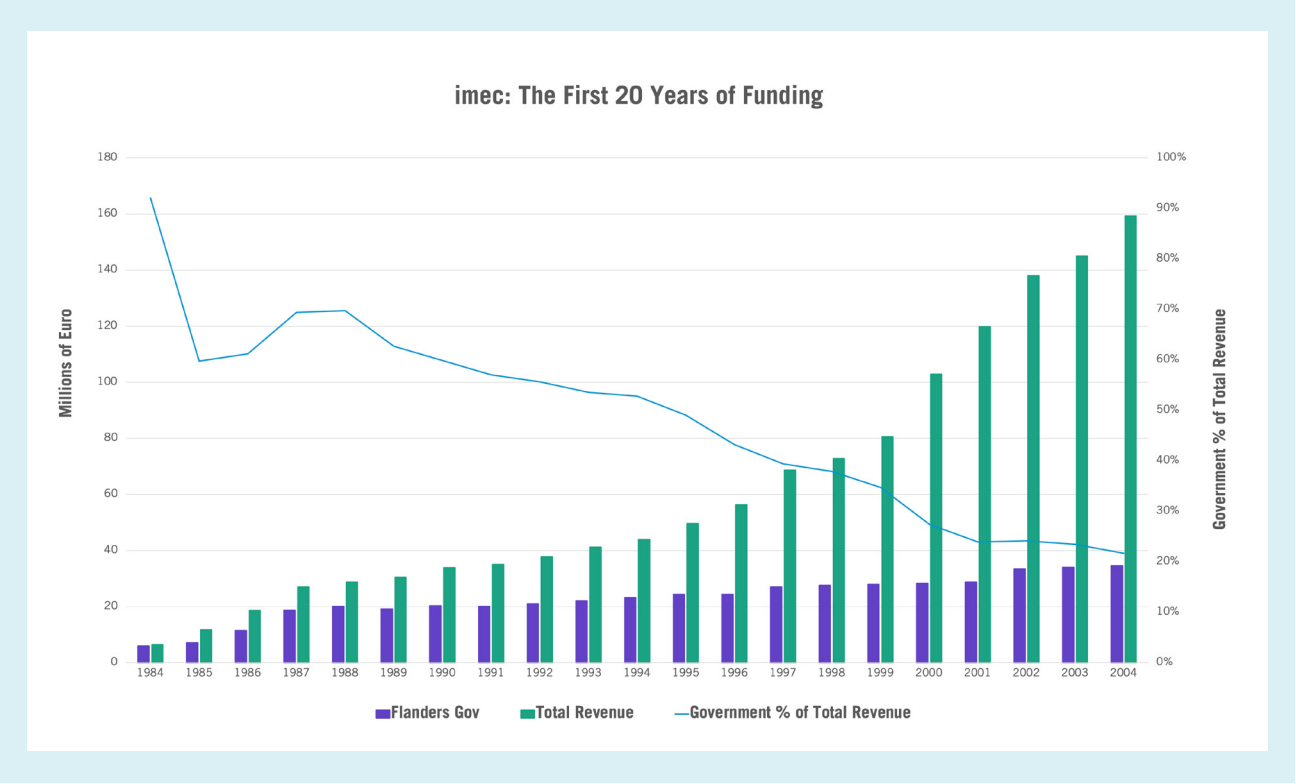


FIGURE 8: IMEC FUNDING OVER ITS FIRST 20 YEARS [16]

Achieving "Financial Sustainability"

Now that we have a frame of reference for what it means for the NSTC to become "financially sustainable," the next step is to examine how the NSTC can create value for the ecosystem and grow diverse revenue streams to achieve such sustainability. In addition to federal government funding, the NSTC should also leverage or attract investments from state and regional entities, as well as bring in revenue from participant dues, fee-for-service work, custom prototyping engagements, investment returns from the venture capital fund, and IP licensing. These income streams will vary widely in size, when they come into play, and how they grow over time. Here, we discuss each of them in chronological order, according to when they come into play for the NSTC, to paint a picture of how the NSTC's financial position and level of sustainability should evolve over time. The NSTC's executive leadership should be accountable for growing these revenue streams and meeting appropriate targets

Federal Government Funding

The first – and largest – source of funding available to the NSTC will be the government's multi-billion-dollar CHIPS Act investment. While initial funding breakouts appear to spread CHIPS Act funding for the NSTC, NAPMP, and related efforts over 5 years (as shown in Figure 8), we recommend spreading that funding over a longer period: roughly 8 to 10 years.

FY22 NDAA	Program	FY22 **	FY23	FY24	FY25	FY26
9906(c)	NSTC	$2.0B	$2.0B	$1.3B	$1.1B	$1.6B
9906(d)	NAPMP	$2.5B				
9906(e)	NIST Metrology	$0.5B				
9906(f)	Mfg USA Institute					

FIGURE 9: INITIAL FUNDING BREAKOUTS FOR NSTC, NAPMP & RELATED EFFORTS IN THE CHIPS AND SCIENCE ACT [17]

While the NSTC certainly will need to make substantial capital expenditures in its first few years to make select, strategic investments in enabling capabilities and infrastructure, it should not exhaust its capital right away. Some enabling capabilities will be critical in the immediate term to support initial Breakthrough Challenge work or to fill long-standing and pressing gaps in the ecosystem, and the NSTC should make aggressive investments to address those gaps (e.g., more accessible design tools, baseline flows, test structures, chiplet platform). However, it is equally critical that the NSTC have resources to address gaps and new pressing needs that may arise later on, after its technical work is well underway and both foreseen and unforeseen roadblocks appear. By making full use of the existing capabilities available in the ecosystem and taking a measured, strategic approach to gap-filling capital expenditures, the NSTC can ensure that it has the resources necessary to address needs that may take a few years to become apparent.

The NSTC – which we recommend be the entity charged with implementing the NAPMP – should leverage a sizable amount of the NAPMP funding to address the critical shortage of packaging R&D and prototyping infrastructure, tools, and capabilities in the U.S. When deploying NAPMP funding both for capital and programmatic expenditures, the NSTC will need to ensure that investments in packaging and other parts of the stack are complementary, mutually-reinforcing, and guided by the technical agenda.

While it may be tempting for the NSTC to front-load investment in Breakthrough Challenges as well, this – like infrastructure and enabling capabilities – is an area where the NSTC should not expect to deploy all of its funds right away. Some potential BTCs may rise quickly to the top of the list and gain widespread buy-in and excitement; the NSTC, naturally, should launch these and begin executing them as soon as possible. The NSTC, however, will not be able to handle as many simultaneous BTCs in year one as it will in subsequent years. The early period of the NSTC's growth will be a time of institutional learning and development, trial and error, and operational refinement. As the NSTC becomes more established, it will be prepared – both strategically and operationally – to ramp up its Breakthrough Challenges to higher funding levels, making more awards and executing a greater number of projects.

Other programs that government funding will support, like the NSTC's workforce development initiatives and venture capital fund, will also begin

** Per the CHIPS and Science Act, the funding for fiscal years 2022 through 2026 is to remain available until expended.

working and creating impact immediately, but will take time to scale. In year one, the NSTC's workforce development team will launch robust outreach and awareness campaigns to educate academic institutions, regional economic development entities, and students about the programs it offers. This will enable the NSTC to develop a broad network of university and community college faculty, regional economic development entities, industry associations, and others that will help recruit and refer students to participate in NSTC programs. Such a network will also be key to executing those programs. By bringing in the right partners early on, the NSTC will be able to attract participants and run high-value programs from the beginning. As word travels around the ecosystem and more people learn about and engage with the NSTC, both the number of students applying for NSTC workforce development programs and the NSTC's ability to support that a growing number of participants will increase. While there will be some fixed costs associated with launching workforce programs, the variable costs associated with participation levels will increase substantially over the first several years, as more and more people become involved in the NSTC's programs. The NSTC's investment of government funds should reflect this. Similarly, an effective venture capital investment arm will take time to refine its sourcing strategy and pipeline of investable companies. It will need to educate partner institutions about its investment thesis and criteria so that they can provide the NSTC with appropriate referrals. While the NSTC will likely find and invest in some compelling deals early on, it must be judicious in how it makes investment decisions. Not all the best ideas and deals will cross its desk right away – the fund's strategy is long-term, and the NSTC needs to make smart investment decisions, not simply fast ones.

Strategic, judicious use of government funding over several years is key to setting up the NSTC for long-term success and financial sustainability in the marathon race for leadership in the global semiconductor ecosystem.

The government will need to make continued, periodic investments in the NSTC to support strategic expansions, the creation and acquisition of new enabling capabilities, and the funding of projects and Breakthrough Challenges that may be of particular interest to government stakeholders. The government should plan to launch a second tranche of funding for the NSTC around year seven so that NSTC leadership can ensure that existing and new programs stay on-course and continue creating impact. If participating organizations and people within the ecosystem perceive that the government is not committed to long-term engagement and investment in the NSTC, they will be less likely to invest in, build careers at, or undertake multi-year projects with the NSTC. Conversely, continuing investment and engagement from the government will be a signal of strength and momentum

Participant Dues

Like government funding, participant dues – i.e., the "entrance fee" that entities will pay to access the NSTC's capabilities and participate in its technical programs – can come into play soon after the NSTC's establishment. Many companies, universities, and other organizations are already eager to engage in the NSTC's work as soon as it launches. Others will be more conservative and will wait to see what capabilities the NSTC will offer, what its initial focus areas will be, and what early results it will generate before they decide to join. Consequently, participant dues will likely ramp up over the first 3-5 years before reaching either a steady state or a more modest rate of growth, as the NSTC captures a substantial portion of its addressable market.

Participant dues will support both technical program execution and the NSTC's general operational costs. Participants should be able to earmark certain portions of their dues to support programs or initiatives that are of interest to them. This will be helpful in presenting a clear, targeted value proposition to participants.

While participant dues will come into play early on in the NSTC's existence, they will not be major revenue drivers. In order to lower barriers to entry and barriers to innovation, the NSTC should have a tiered structure for dues that allows organizations of all sizes and stages to participate in its work.

State and Regional Entity Investments

As the NSTC begins stitching together its network of infrastructure across the country, making initial investments in enabling capabilities, and launching its workforce development programs, it quickly will attract attention from state and regional entities eager to grow the industrial footprint and talent base in their respective areas. There will likely be a burst of investment from states and regional entities in the NSTC's first few years, which may take the form of grants for or co-investments in workforce development programs, subsidies for infrastructure, etc. As this happens, it will likely motivate other states and regional entities to make similar investments. As the NSTC continues to evolve and invest in more enabling capabilities over time, there will likely be additional periodic investments from state and regional entities throughout the country. These investments may arise opportunistically and be tied to particular programs or capital expenditures, rather than being sources of continuous, unrestricted income.

Fee-for-Service and Custom Prototyping Engagements

The NSTC's largest, and most important, source of private-sector revenue will come from fee-for-service and custom prototyping engagements. As the NSTC invests in critical gap-filling enabling capabilities, as well as in tools that help participants locate and access specific capabilities and resources throughout its network, it will become a go-to partner for innovators from all sectors within the ecosystem. Innovators will be willing to pay to utilize unique capabilities at the NSTC on a fee-for-service basis. Additionally, participants increasingly will see the unique value that comes from collaborating with others, prototyping, and scaling innovations at the NSTC, and will be willing to pay to have their own, custom projects prototyped and demonstrated at the NSTC. This type of offering has been valuable to the growth of imec, and it will be instrumental in the growth of the NSTC as well, though the NSTC will tend to focus later in the MRL scale.

It will take a couple of years for the NSTC to begin generating notable revenue from fee-for-service and custom prototyping engagements. As the NSTC continues to invest in new, unique enabling capabilities and demonstrates the success and value of its work, it will be able to attract more new and repeat business. While these direct, paid engagements with participants will, together, constitute the largest, consistent private revenue stream for the NSTC, they will never match the levels of initial government funding provided by the CHIPS Act.

IP Licensing

As the NSTC's technical programs generate intellectual property, the NSTC will be able to license some of it in exchange for revenue. Because the NSTC will be focused on revolutionary, next-generation technology and will be focused on high-risk, high-reward projects, it will likely take several years to generate licensable IP. Even after the NSTC has developed a portfolio of licensable IP, the revenue it derives from licensing will likely be small compared to other revenue streams. For reference, A*STAR which was established over 30 years ago, reported 2022 licensing revenue of approximately $17 million SGD (roughly $12.5 million USD), while reporting industry revenues of $481.5 million SGD (roughly $355 million USD).[18] The NSTC's licensing revenue initially will be much lower than that as it builds its IP portfolio.

Venture Capital Fund Returns

In addition to earning revenue from its technical work, the NSTC, eventually, also will bring in revenue from its venture capital fund. Assuming that the NSTC's venture capital fund begins making investments in year one and that, on average, time-to-exit is longer than the typical venture capital time horizons, the NSTC can expect to begin seeing returns around the 10-year mark.[11] As with any venture fund, the amount of money that investments generate will vary substantially. In order for the fund to be sustainable over time, it will need to reinvest at least some of its income.

Years 1 - 5	Years 6 - 10	Years 11+
• In the first year, nearly all funding comes from CHIPS Act • Participation fees begin in year one but grow substantially over this period • By the end of this period, the NSTC is generating notable revenue from fee-for-service engagements • State and regional entities support infrastructure projects and workforce development programs in their areas, either through grants or co-investments	• CHIPS Act funding continues to support acquisition/creation of enabling capabilities and new infrastructure, as needed • Participation fees begin to top-out as the NSTC nears maximum ecosystem participation • Fee-for-service custom prototyping engagements are now a substantial portion of revenue, but have not tipped public-private funding balance toward majority private • States and regional entities continue to make opportunistic investments in infrastructure, projects, and programs in their areas	• Initial CHIPS Act funding already fully deployed; federal government continues to provide funding support, albeit at lower levels • Fee-for-service work continues to grow, driving private-sector revenue • First successful exits from investment fund bring in revenue • Participation fees are fairly stable • IP licensing income picks up, but remains low overall • Every few years, states and regional entities fund or co-invest in NSTC projects in their areas ***By years 15-20, NSTC may reach 70:30 ratio of private revenue to government funding***

FIGURE 10: STAGES OF THE NSTC'S FINANCIAL DEVELOPMENT

The key to ensuring that the NSTC is able to diversify its income streams successfully, as we describe here, is providing clear and enduring value to its participants. Breakthrough Challenges need to be inspiring, high-impact, full-stack, and inclusive of players throughout the ecosystem. They need to serve the objectives of both the private sector and critical government stakeholders, as well as open up new markets. The NSTC's work must be whole-of-nation, so that states, regional entities, educational institutions, and companies throughout the country see roles for themselves and are motivated to invest in the NSTC's success. The NSTC must provide differentiated value to innovators so that it becomes a go-to resource for any innovator in the ecosystem – whether from industry, government, or academia – that needs to access special capabilities to prototype and to scale their technologies. It needs to catalyze innovation in the ecosystem by sharing the IP it generates through licensing and by making venture capital investments in promising startups as well. When the NSTC takes this multi-faceted approach to value-creation for the whole ecosystem, it will naturally attract greater investment from the private sector and other non-federal sources. In this context, continuing, long-term support from the federal government will provide valuable shots of fuel and energy that will bolster the NSTC's ability to continue running quickly and smartly toward ever-stronger leadership in the global semiconductor ecosystem.

Conclusion

The passage of appropriations for the CHIPS Act has the potential to be a crucial inflection point in not only the history of the U.S. semiconductor industry, but of U.S. technology leadership writ large. However, with adversaries and allies making significant investments as well, there is a risk that – if not leveraged strategically – the U.S. ecosystem's surge in investment ultimately could be simply table stakes. To gain and maintain the lead in the race for global semiconductor leadership, the U.S. needs to treat the NSTC as a long-term endeavor that requires sustained commitment, not as a one-and-done infusion of resources. In this paper, MITRE Engenuity and The Semiconductor Alliance provide a blueprint for how the DOC can ensure that the NSTC is an enduring national resource that will advance U.S. semiconductor leadership for decades to come. While we organized our blueprint into sections about effective governance, setting high-impact technology agendas, creating the network and operational model that will enable the NSTC to execute its work successfully, and achieving financial sustainability, we want to close by emphasizing the key cross-cutting themes that underpin all of our recommendations: stewardship, inclusivity, and ambition.

Stewardship

The NSTC will have a great responsibility to the nation to adhere to its mission above all else and to create maximum impact with the resources entrusted to it. It is for this reason that, both here and in our previous paper *American Innovation, American Growth: A Vision for the National Semiconductor Technology Center*, we began our recommendations with deep explorations of governance. It is also why we strongly recommend that the NSTC be responsible for executing the NAPMP; placing both the NSTC and the NAPMP under a single governance structure will not only advance innovation and technology outcomes by enabling leadership to drive full-stack approaches across all work, but it will eliminate needless duplication of overhead that would detract from their technical missions. The importance of good stewardship is also a key driver behind our recommendations that the NSTC leverage the wide set of capabilities that already exist throughout the country and invest regularly in new enabling capabilities that drive value for all participants. When the NSTC demonstrates good stewardship and strong commitment to value creation, it will attract continued investment from all sectors of the ecosystem, turning the initial "seed" planted by the DOC and NIST into a flourishing, enduring national resource.

Inclusivity

In order to maintain a competitive edge on the global stage, the U.S. needs to bring the collective strength of its whole ecosystem to bear on challenges of national importance. The seeds of tomorrow's groundbreaking technologies lie in both established, industry-leading companies and emerging startups. All of the components of future systems – that is, the various elements of the full stack that must come together to make future technologies possible – will come from a diverse range of companies that all have unique expertise, capabilities, and innovations. Government agencies, national labs, and the defense industrial base have highly specialized expertise and capabilities that are critical to our national security. Academic institutions and industry organizations are at the forefront of R&D, driving innovation and discovery that will shape and enable the technology of the future. All of these facets of

the ecosystem must have a place in the NSTC, and the NSTC must leverage their unique contributions of each to maximum effect. The NSTC must dedicate itself to a whole-of-nation, full-stack approach to innovation in order to advance U.S. leadership over the long term.

Ambition

While the NSTC must always be a good steward of the resources entrusted to it, it cannot achieve its mission of driving the lab-to-fab transition of revolutionary technology in the U.S. by being conservative or risk averse. The NSTC needs effective frameworks, the right set of experts, decision-makers, and advisors, and insight into market needs in order to create marketing shaping high-impact Breakthrough Challenges. An ambitious appetite for taking smart risks is key to ensuring that the NSTC aims high when it comes to defining and executing its technology agendas. The NSTC must be ambitious with respect to its own evolution and growth as well. While we recommend that the NSTC start by leveraging a network of existing facilities and capabilities throughout the country to execute its work, this is not enough to ensure future success. Rather, the NSTC must create value for the U.S. ecosystem. The NSTC will do this by investing regularly in new, unique enabling capabilities that attract innovators from all segments of the ecosystem. Over time, with continued strategic investment, many of the hubs, spokes, and annexes in the NSTC's network can become truly world-class, peerless centers of gravity for innovation across various aspects of semiconductor technology. The NSTC should aspire to be an unparalleled national treasure.

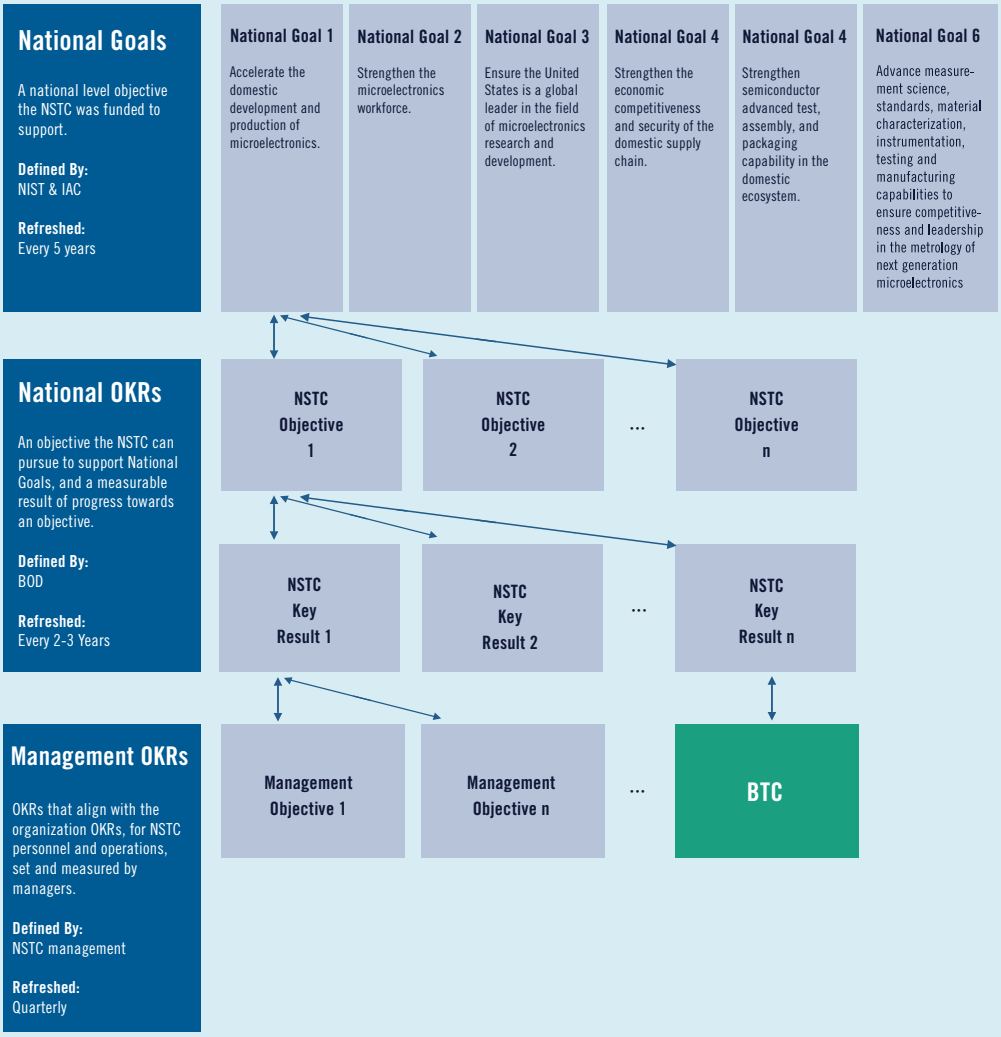
We titled this paper a "blueprint" because it describes a robust outline and foundation for the NSTC, but still leaves several important details to be defined. There are also some important topics which we did not address in detail here – particularly workforce development and the operations of the NSTC's venture capital fund – that are worthy of their own papers. The work of the American Semiconductor Academy and SEMI already provides a deep understanding of the challenges and solutions to workforce development.[19] We firmly believe that the technology, workforce development, and investment functions of the NSTC are tightly interrelated and should be closely aligned to the NSTC's efforts to ensure that they are mutually reinforcing and utilize resources efficiently to generate maximum impact. We hope that this "blueprint" serves as an invitation to engage in a deeper national conversation about how all segments of the U.S. ecosystem can contribute to making the NSTC an enduring national resource that gives the U.S. a sustained advantage in the race for global leadership in semiconductors for decades to come.

Appendix

In the Governance section above, core values were outlined and a system for setting and measuring objectives of the NSTC was referenced. This section will describe that system in more detail, along with proposed examples.

We propose three levels of goals for managing the NSTC. These three levels, and how they interlock with each other, are illustrated in in the diagram below.

Objectives Framework for the NSTC and NAPMP



National Goals: The NSTC must define the national level and strategic goals that it was founded to address. To ensure the goals continuously align with the needs of the nation, while avoiding the pressures of the short-term market and political dynamics, these goals should be re-evaluated every 5-7 years by the Department of Commerce and Industrial Advisory Committee. These goals should be initialized using the legislated mandate in the 2021 National Defense Authorization Act, which specifies the six national goals of the CHIPS Act:

1. Accelerate the domestic development and production of microelectronics.
2. Strengthen the microelectronics workforce.
3. Ensure the United States is a global leader in the field of microelectronics research and development.
4. Strengthen the economic competitiveness and security of the domestic supply chain.
5. Strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem.
6. Advance measurement science, standards, material characterization, instrumentation, testing, and manufacturing capabilities that ensure competitiveness and leadership in the metrology of next generation microelectronics.

NSTC Objectives and NSTC Key Results: These are high level objectives and key results that encompass the work the NSTC will take to support the national goals. Each national goal will have one or more NSTC objective tied to it. Establishing the NSTC objectives will lay out the roadmap of institution-level actions over a 3 -5-year time horizon. These should be reviewed, graded, and updated on an annual basis. NSTC objectives are set and measured by the Board of Directors and NSTC executives, in order to include a wide level of stakeholders from industry, academia, and government. Below is an example NSTC objective for illustrative purposes.

An example NSTC objective, that serves the second national goal, strengthening the microelectronics workforce, would be:

> *Increase the work pool of fab-ready technicians.*

And a supporting NSTC key result for this objective would be:

> *Train 300 technicians over 3 years in fab operations.*

Management Objectives and Management Key Results: These objectives and key results should be set at the NSTC Management level and will be the framework for managing projects and day-to-day operations of the organization. Each objective and key result will accrue up to an NSTC key result. Breakthrough Challenges would be one example of a technical goal that would be set by the NSTC Management and the Technical Advisor Committees. As a useful reference, The Semiconductor Alliance has developed a set of example management key results that could be considered by the NSTC Management.

	Suggested Management Objectives and Key Results	Suggested NSTC Objectives and Key Results
Operations		
	The number of: • BTC's and projects brought to commercial production • Members, dues paid • Projects delivered on schedule • Academic and commercial research partnerships started	• The ratio of revenue from public / private sources • The turnaround time for project iterations
Workforce		
	The number of: • BS, MS, and PhD in *Targeted Degree* programs • Students hired by the semiconductor industry • Semiconductor focused academic programs • Semiconductor focused training programs	• The rate of US citizen students graduating in relevant 2-year technical programs and 4-year academic programs • The geographic, economic, racial diversity of trainees • Targeted Degree programs: ChemE, CompE, CS, EE, MatSci, Physics
Technical		
	The number of: • Technologies, processes, and products transferred to commercial production domestically • Patents developed and licensed • Peer reviewed papers and conference presentations	• Dollars of licensing revenue generated • Change in industry roadmap acceleration
Economic		
	The number of: • Jobs indirectly created in downstream industries • Semi start-ups founded, funded, acquired, and IPO'd • Supply chain companies engaged with the NSTC	• The portion of DIB supply chain domestically produced • Opening of markets for new industries (e.g., EV, medical, etc.)

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